Embedded Systems Lab 2 - HS 2020

14.10.2020

Zhongnan Qu

Lab structure

- **Goal of today's lab:**
  - Get to know hardware interrupts and hardware timers.
- **Agenda:**

Wednesday	16:15 - 18:00	Introduction (recorded) and questions
Friday	16:15 - 18:00	Questions & Answers

- **Available assistants:**
  - Zhongnan Qu - TA
  - Michael Lustenberger - SA
  - Luca Rufer - SA

Lab structure

- **Interactions:**
  - **Exercise Zoom:** Questions can be asked throughout the lab in this room by raising your hand. Please feel free to write in the chat in case we oversee your question.
  - **Help Zoom:** Student assistants are available throughout the session for 1-on-1 meetings under the Zoom Meeting ID 917 6971 5701.
  - **Matrix Chatroom:** Questions that are relevant for everyone can be asked in the Matrix chatroom where the responsible assistants can answer as quickly as possible.
  - **In-person:** Students can come to ETZ D96 to ask questions in person.

Goals of this Lab

- Configuration of **hardware interrupts**
- Interrupt vs. Polling
- Learn how to **debug** program running on a microprocessor
- Configuration of **hardware timers**
- Implementation of **pulse-width modulation (PWM)**

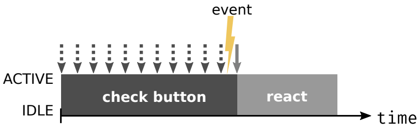
Hardware Interrupt

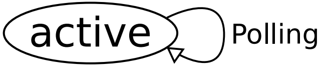
Definition

A *hardware interrupt* is an electronic signal that alerts the microprocessor of an event. An interrupt can be triggered by either an internal peripheral (e.g. timer) or an external device (e.g. button).

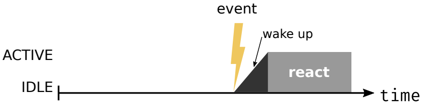
Polling vs. Interrupts

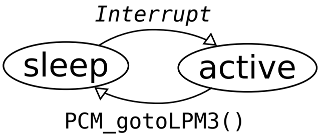
Polling



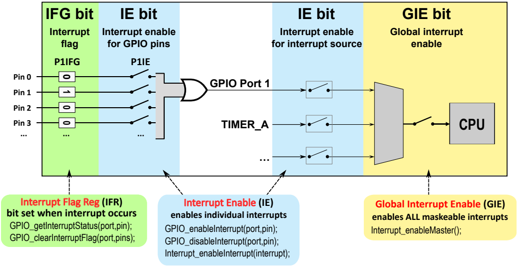


Interrupts





Setting up an Interrupt



Interrupt Flag Reg (IFR)
bit set when interrupt occurs
GPIO_getInterruptStatus(port,pin);
GPIO_clearInterruptFlag(port,pins);

Interrupt Enable (IE)
enables individual interrupts
GPIO_enableInterrupt(port,pin);
GPIO_disableInterrupt(port,pin);
Interrupt_enableInterrupt(interrupt);

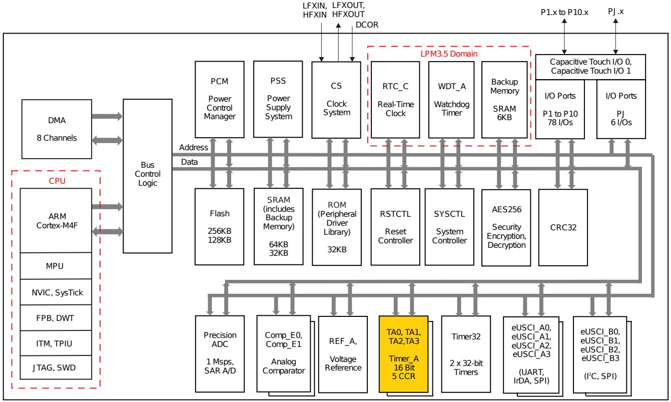
Global Interrupt Enable (GIE)
enables ALL maskeable interrupts
Interrupt_enableMaster();

1. Enable interrupt for GPIO pin
2. Enable interrupt source (GPIO port)
3. Globally enable interrupts

- **Interrupt service routine (ISR):** Special “function” which is executed when a specific interrupt is triggered

ETH zürich

Hardware Timer



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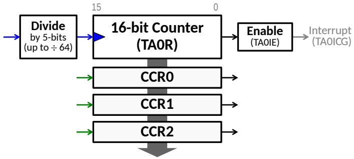
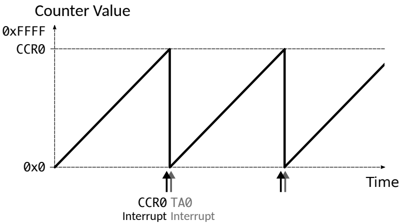
- Timer_A (TA): internal peripheral of the MSP432.
- 4 instances:
  `TA0`, `TA1`, `TA2`, `TA3`

Hardware Timer

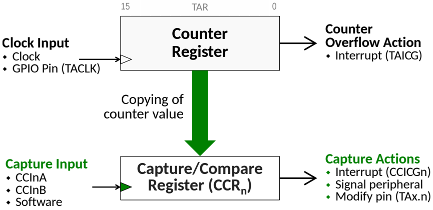




- **Counter**: Main component, incremented on every input edge
- **Divider**: Divides the input clock signal
- **CCR**: Registers to control the timer's behavior.
- **Counting modes**:
  - Continuous
  - Up (used in this lab)
  - Up/Down
- **Output:** interrupt, modify pin, signal to peripheral

Capture and Compare

Input Capture



15 TAR 0

Counter Register

Clock Input
- Clock
- GPIO Pin (TACLK)

Counter Overflow Action
- Interrupt (TAICG)

Copying of counter value

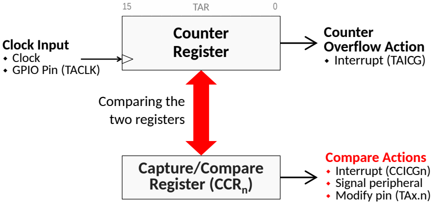
Capture Input
- CCInA
- CCInB
- Software

Capture/Compare Register (CCR_n)

Capture Actions
- Interrupt (CCICGn)
- Signal peripheral
- Modify pin (TAx.n)

If an event occurs, the current counter value is stored in the CCR register (and optionally another event is triggered).

Output Compare



15 TAR 0

Counter Register

Clock Input
- Clock
- GPIO Pin (TACLK)

Counter Overflow Action
- Interrupt (TAICG)

Comparing the two registers

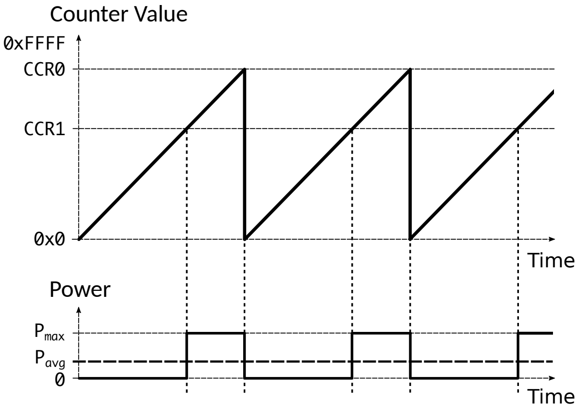
Capture/Compare Register (CCR_n)

Compare Actions
- Interrupt (CCICGn)
- Signal peripheral
- Modify pin (TAx.n)

Triggers an action if the counter value equals the CCR register value.

Pulse-width Modulation (PWM)

- Switch a load on and off at a high frequency
- *Average* transferred power can be configured with the duty-cycle in software



Tasks of Lab 2

- Task 1:
  - Interrupts
  - Debugging
- Task 2:
  - Timers
  - PWM

Introduction is over. Feel free to ask questions!

- The assistants are now available **until 18:00** to answer questions.
  - **Zoom:** Either ask in this channel or use the Zoom Meeting ID 917 6971 5701 to talk individually with an assistant.
  - **Matrix-Chatroom:** Ask a question in the chatroom so other students can also profit from the response (or respond even quicker!)
  - **Email:** For individual questions, you can also reach me under `zhongnanqu@ethz.ch`.
- On **Friday from 16:15 - 18:00**, we will also be available for questions.

Happy coding!

Questions?

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