

Embedded Systems

8. Hardware Components

© Lothar Thiele

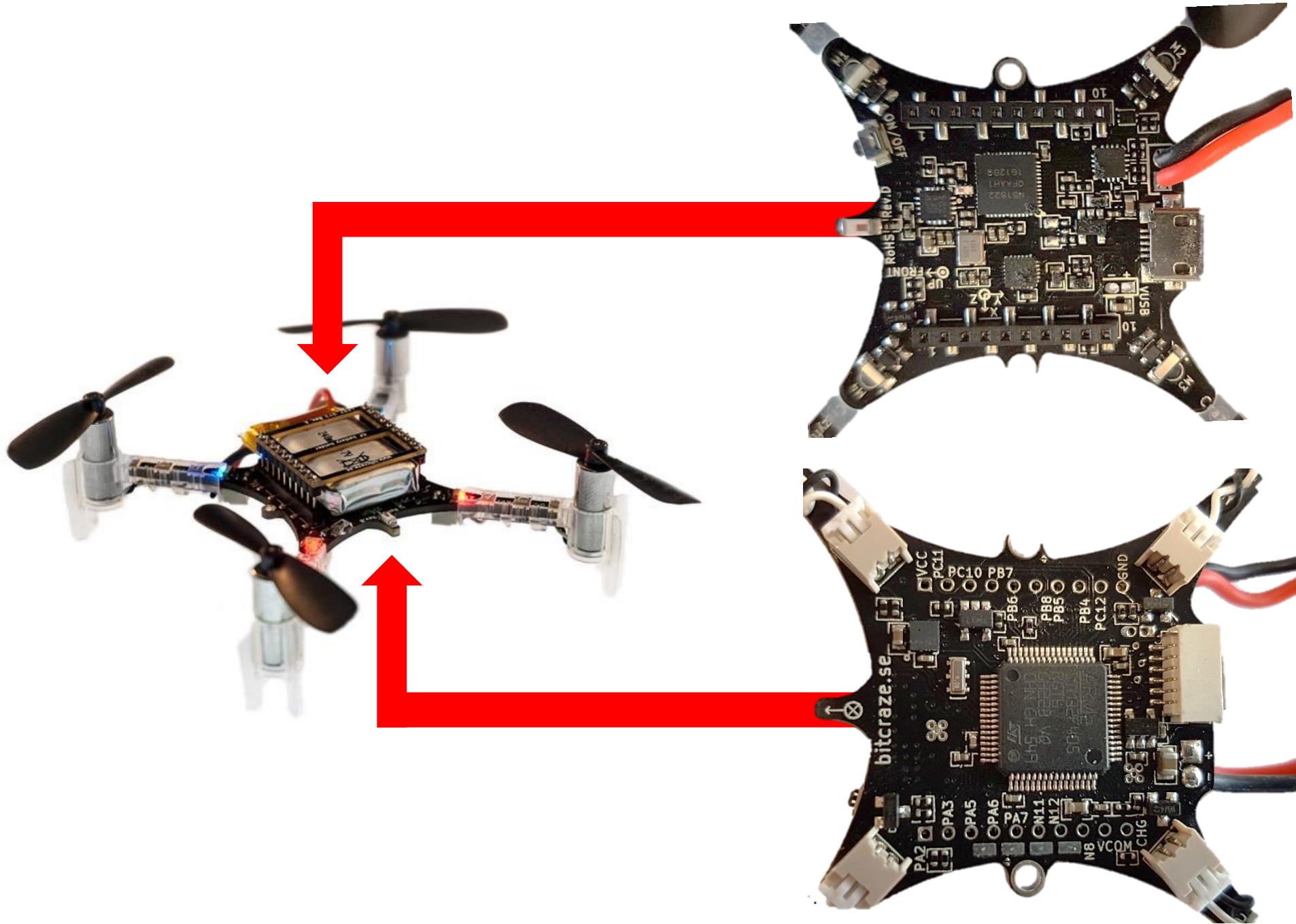
Computer Engineering and Networks Laboratory



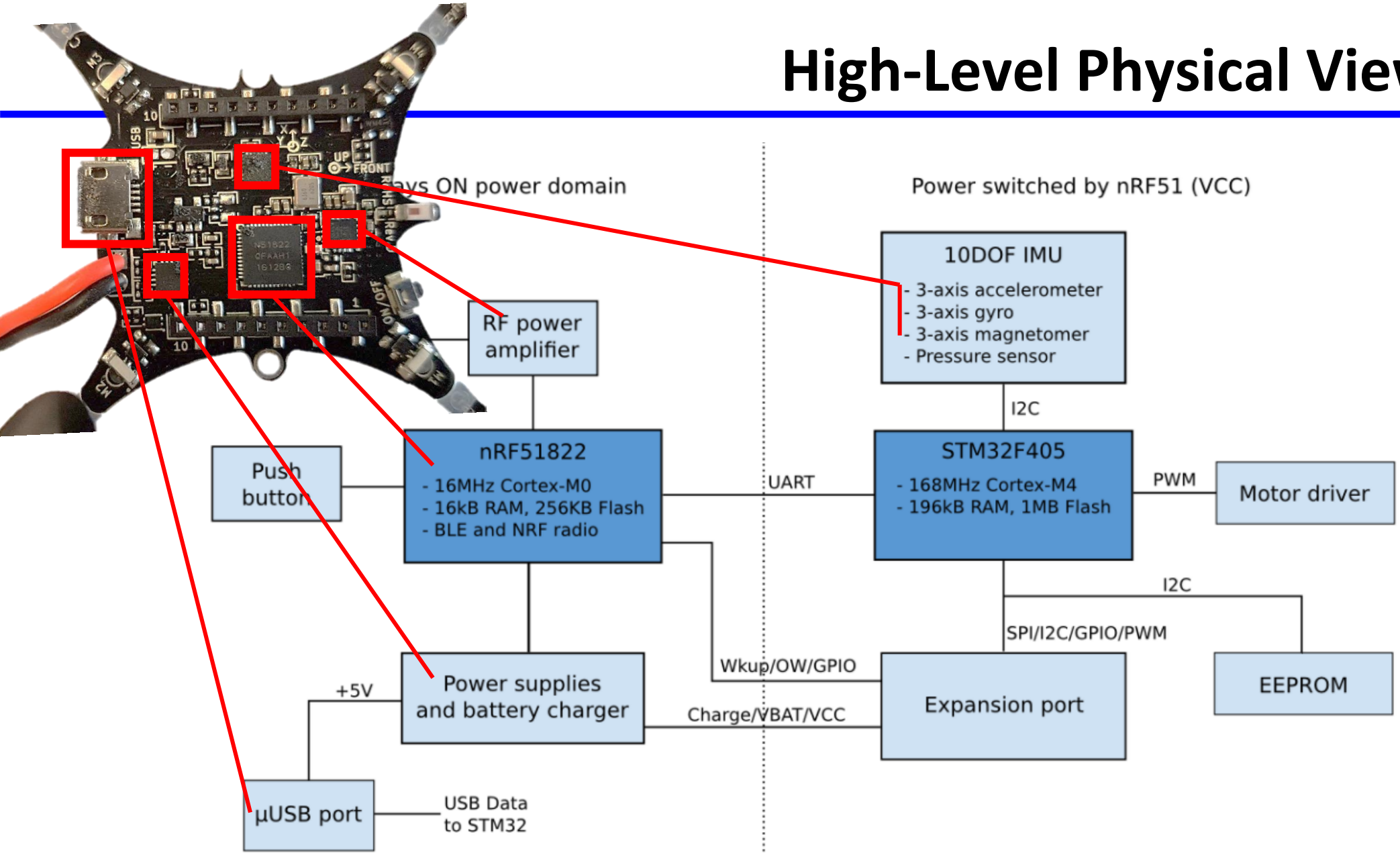
Where we are ...



Do you Remember ?

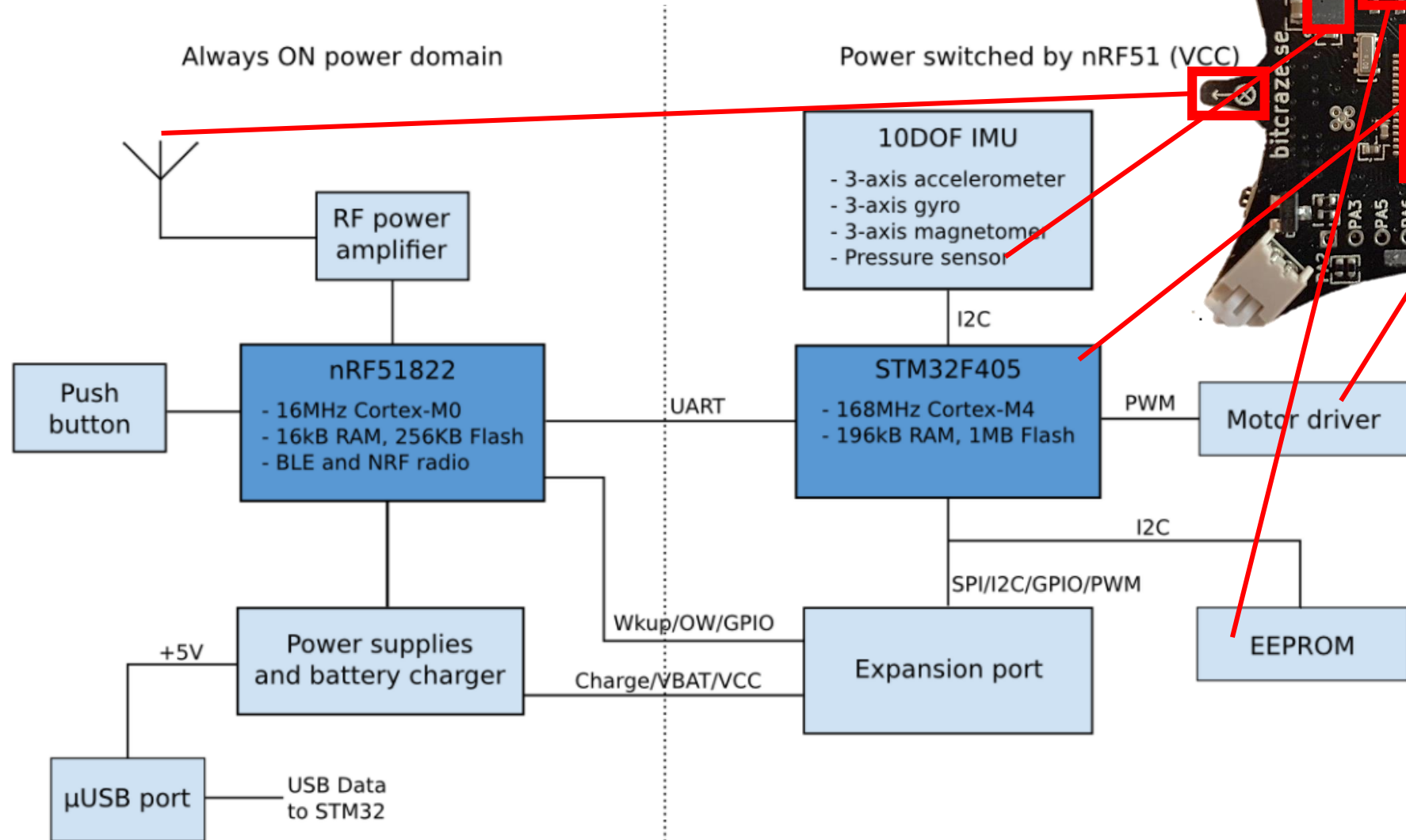


High-Level Physical View



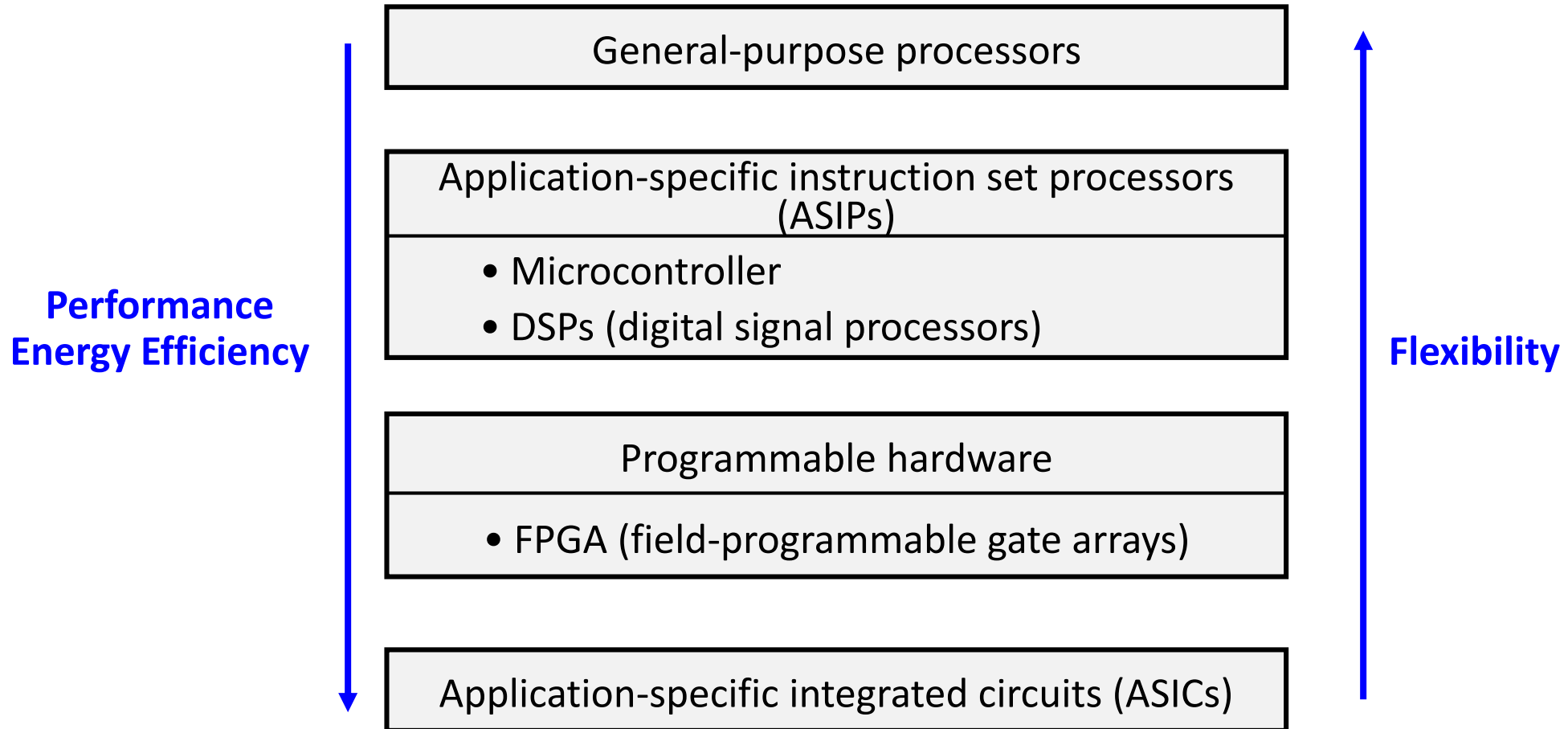
Crazyflie 2.0 system architecture

High-Level Physical View

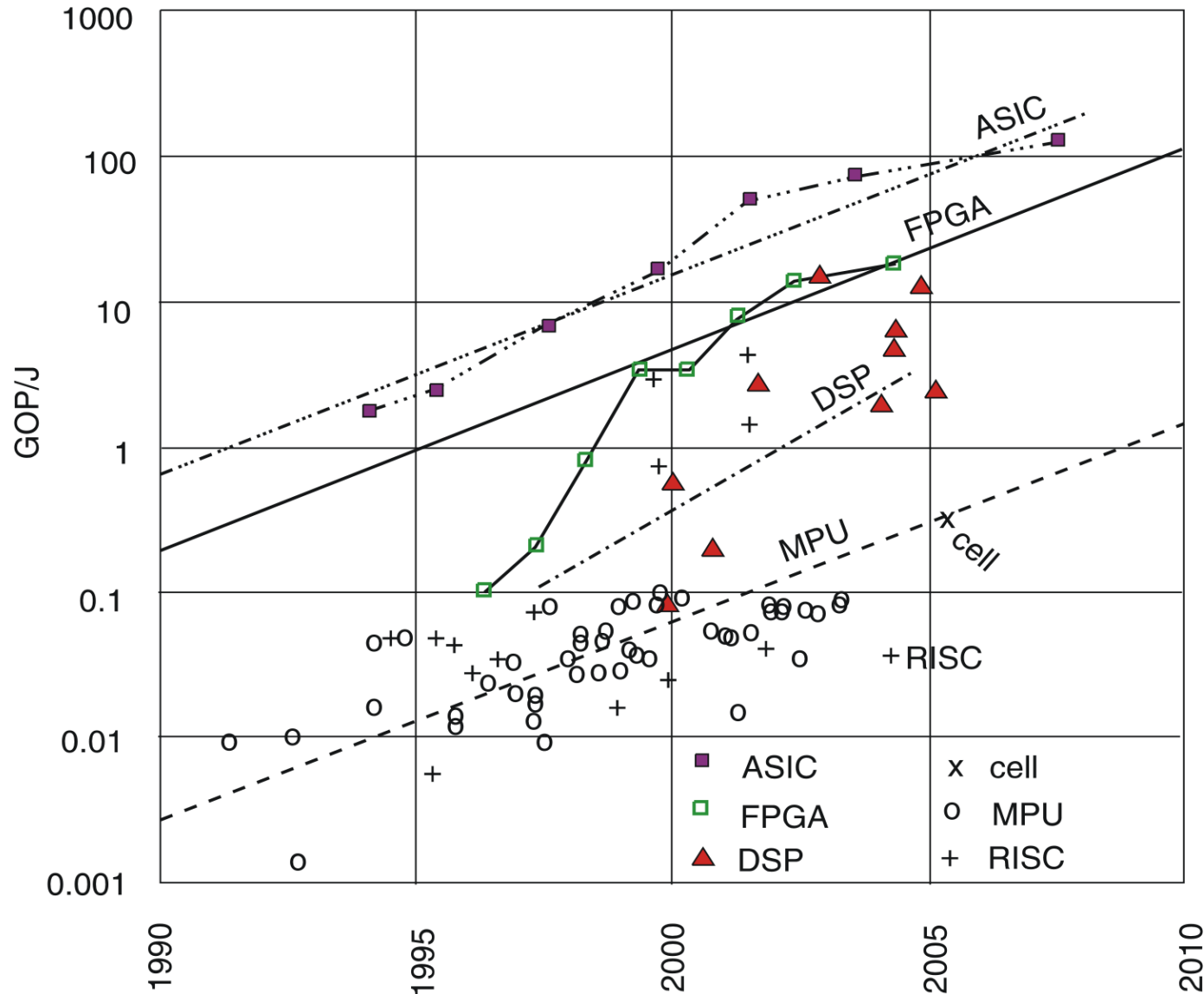


Crazyflie 2.0 system architecture

Implementation Alternatives



Energy Efficiency



© Hugo De Man, IMEC,
Philips, 2007

Topics

- **General Purpose Processors**
- System Specialization
- Application Specific Instruction Sets
 - Micro Controller
 - Digital Signal Processors and VLIW
- Programmable Hardware
- ASICs
- System-on-Chip

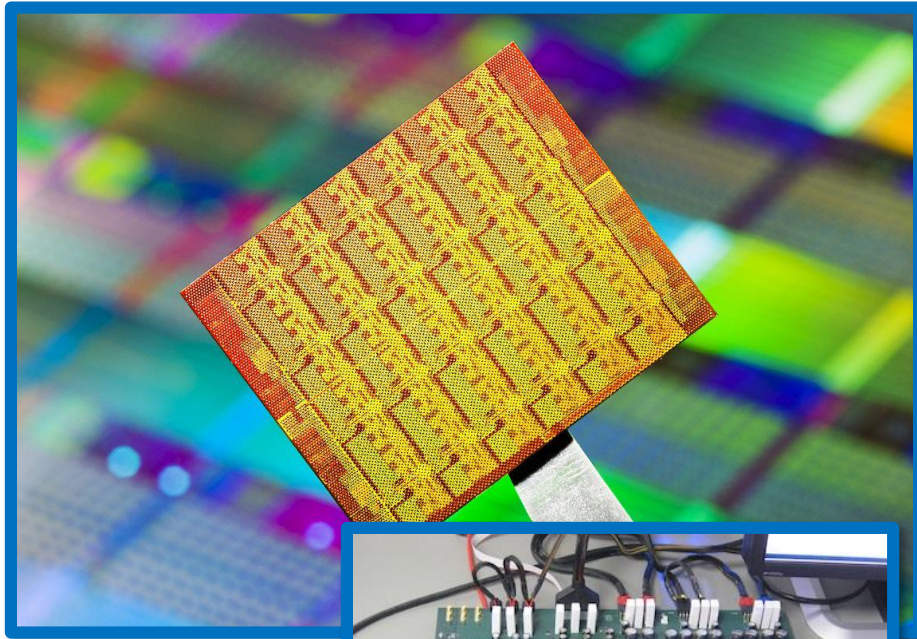
General-Purpose Processors

- *High performance*
 - Highly optimized circuits and technology
 - Use of parallelism
 - superscalar: dynamic scheduling of instructions
 - super-pipelining: instruction pipelining, branch prediction, speculation
 - complex memory hierarchy
- *Not suited for real-time applications*
 - Execution times are highly unpredictable because of intensive resource sharing and dynamic decisions
- *Properties*
 - Good average performance for large application mix
 - High power consumption

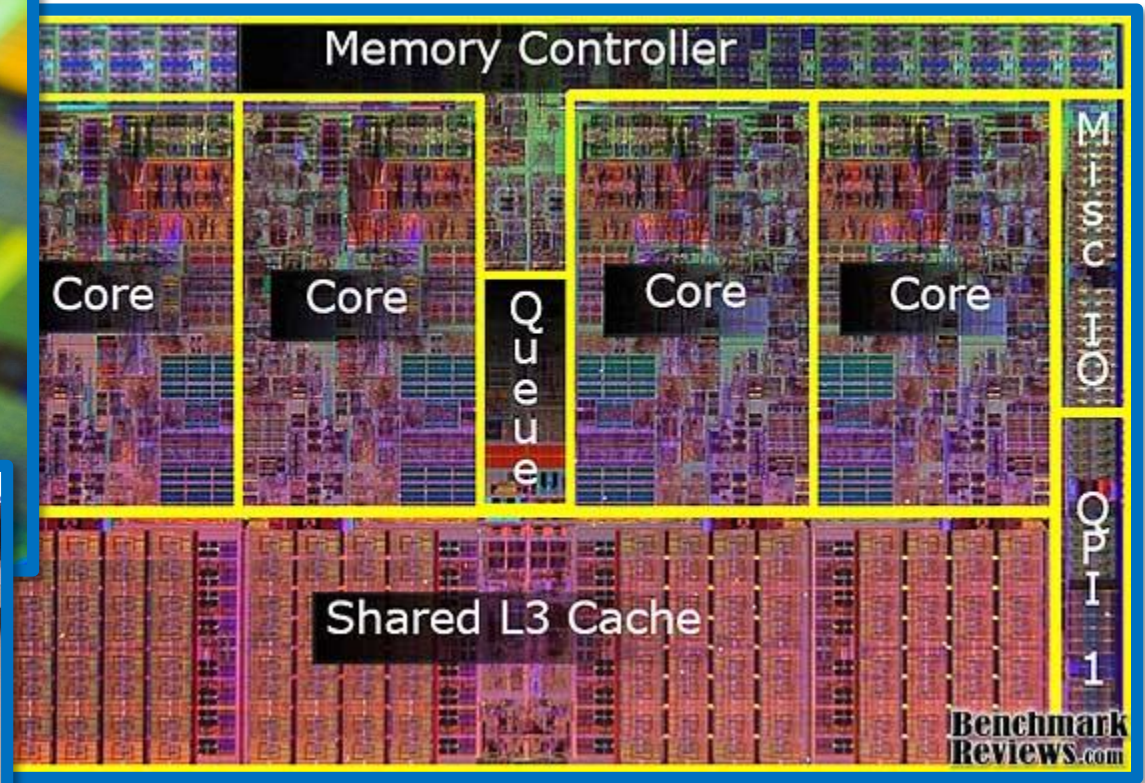
General-Purpose Processors

- *Multicore Processors*
 - Potential of providing higher execution performance by exploiting parallelism
 - Especially useful in high-performance embedded systems, e.g. autonomous driving
- *Disadvantages and problems* for embedded systems:
 - Increased interference on shared resources such as buses and shared caches
 - Increased timing uncertainty

Multicore Examples

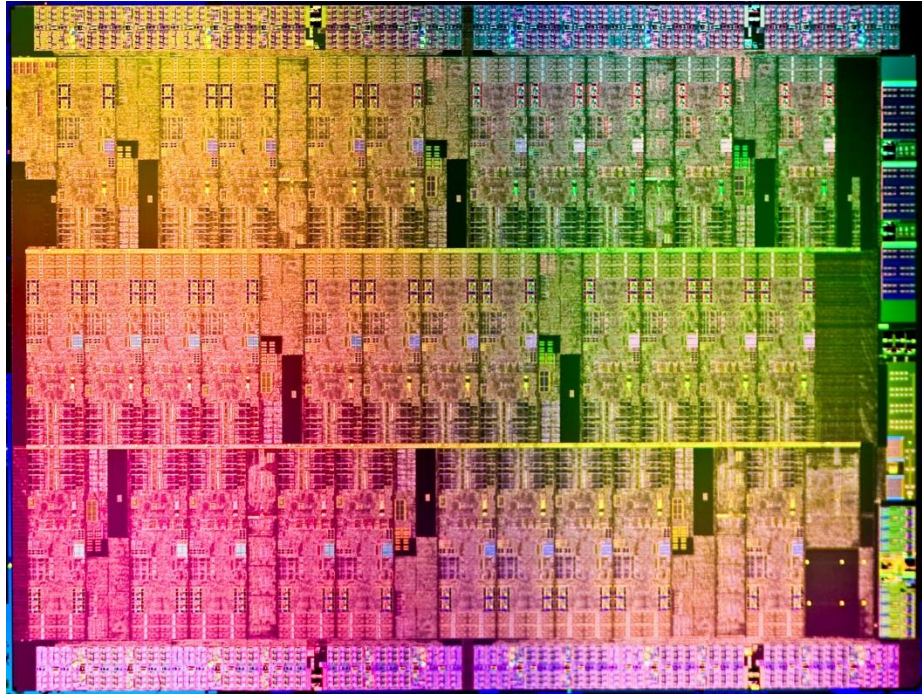


48 cores

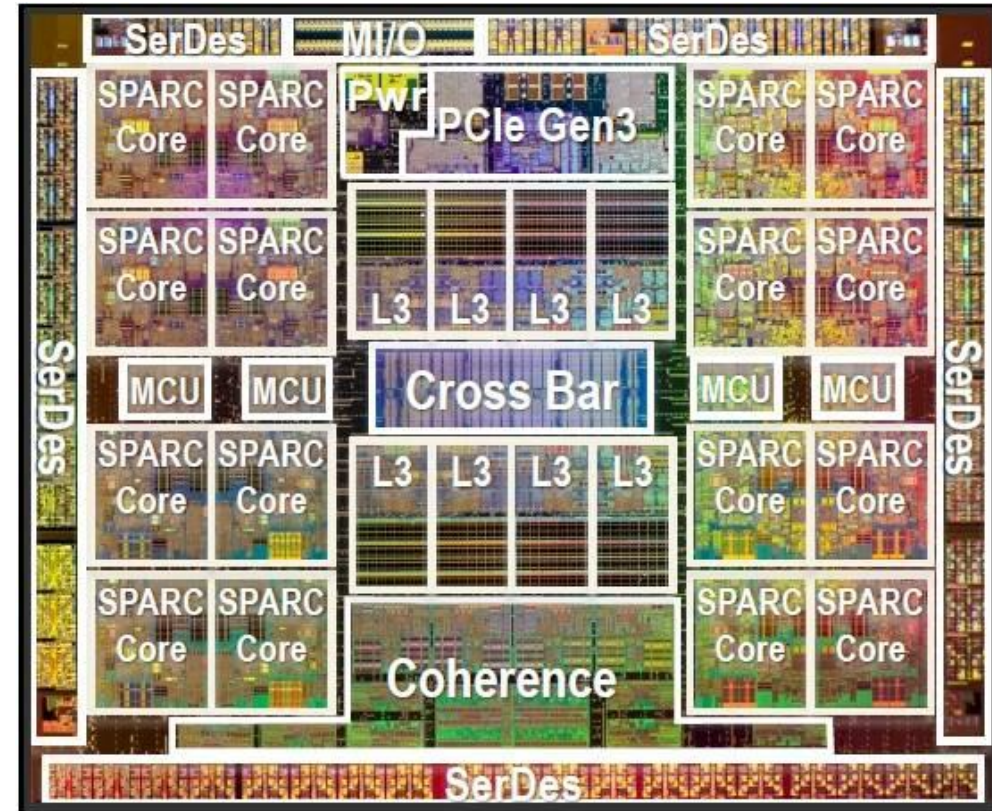


4 cores

Multicore Examples

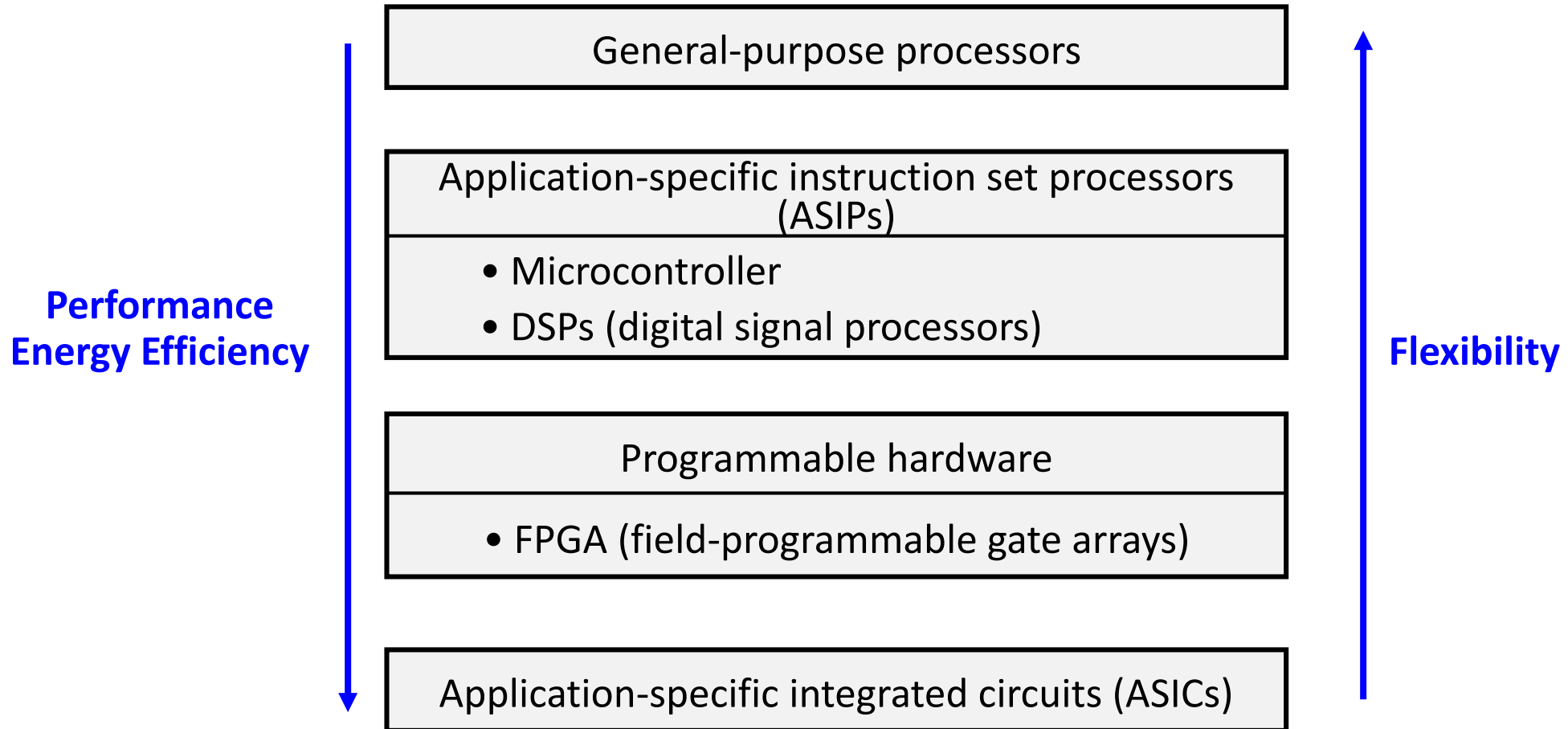


Intel Xeon Phi
(5 Billion transistors,
22nm technology,
350mm² area)



Oracle Sparc T5

Implementation Alternatives



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- Heterogeneous Architectures

System Specialization

- The main difference between general purpose highest volume microprocessors and embedded systems is *specialization*.
- *Specialization should respect flexibility*
 - application domain specific systems shall cover a class of applications
 - some flexibility is required to account for late changes, debugging
- *System analysis required*
 - identification of application properties which can be used for specialization
 - quantification of individual specialization effects

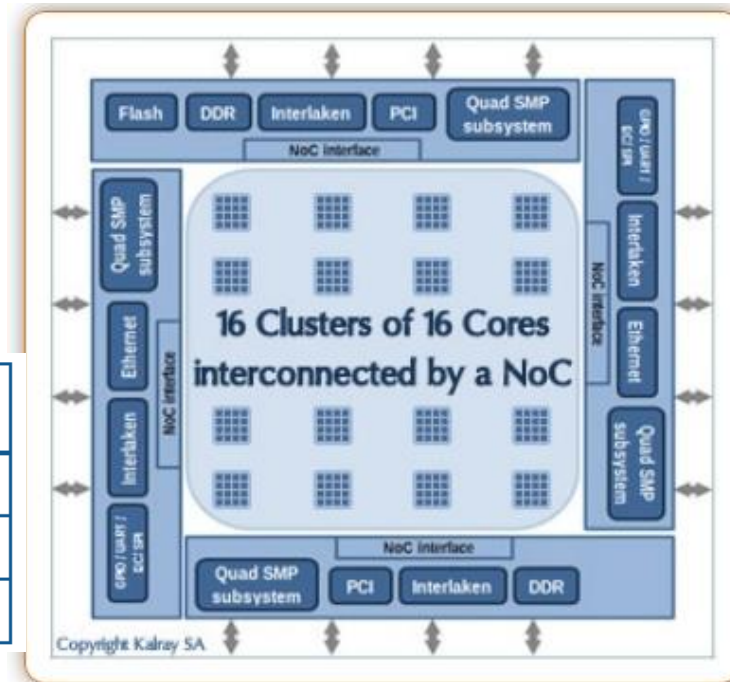
Embedded Multicore Example

Recent development:

- Specialize multicore processors towards real-time processing and low power consumption
- Target domains:

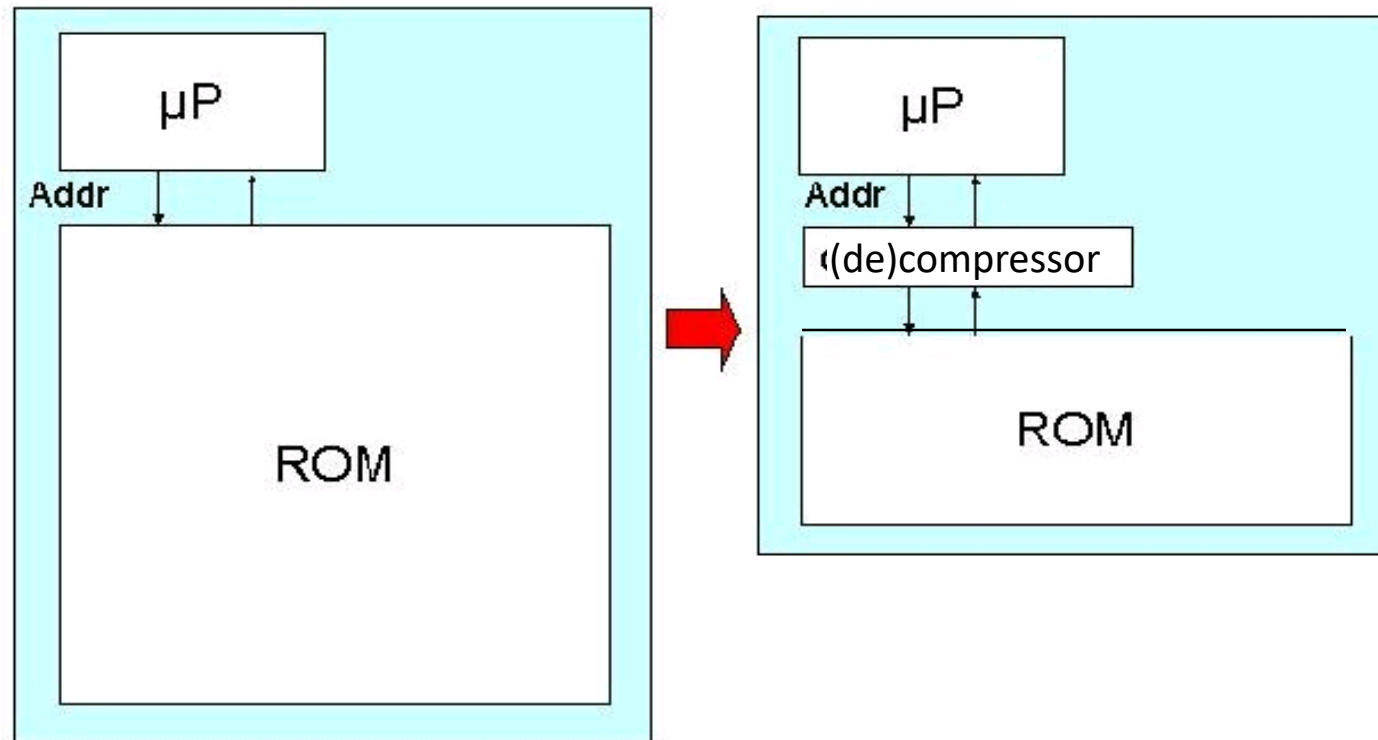


| Core Generation | Number of Processing Cores | GFLOPS/W | GOPS/W |
|-----------------|----------------------------|----------|--------|
| Andey | 256 | 25 | 75 |
| Boston (2014) | 256 | 50 | 80 |
| Coolidge (2015) | 64/256/1024 | 75 | 115 |



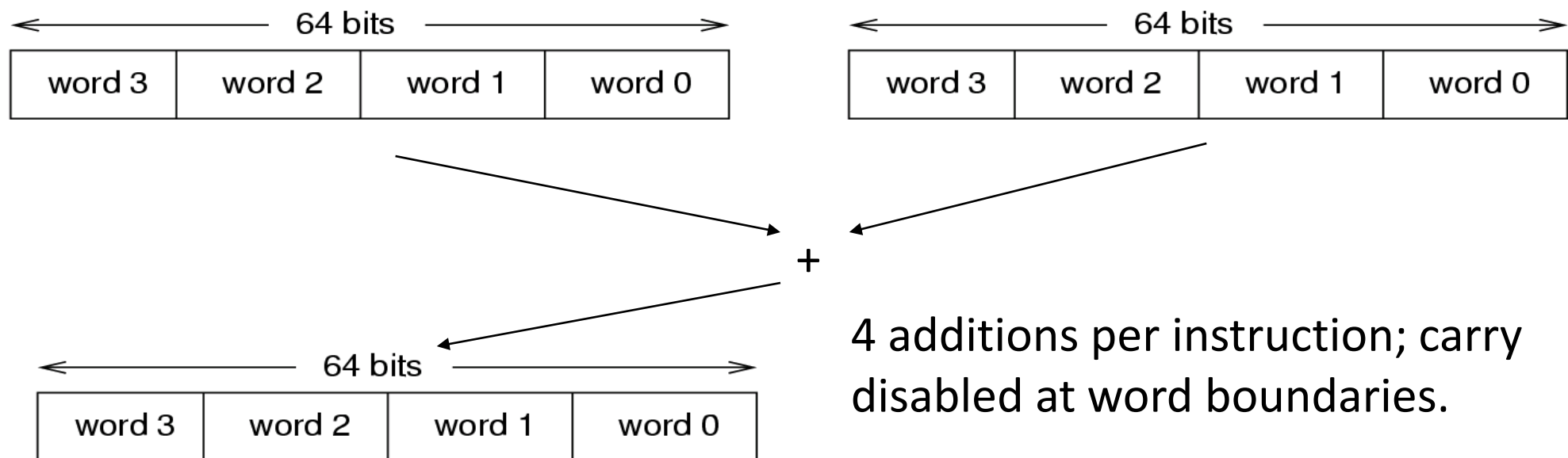
Example: Code-size Efficiency

- RISC (Reduced Instruction Set Computers) machines designed for run-time-, not for code-size-efficiency.
- *Compression techniques*: key idea



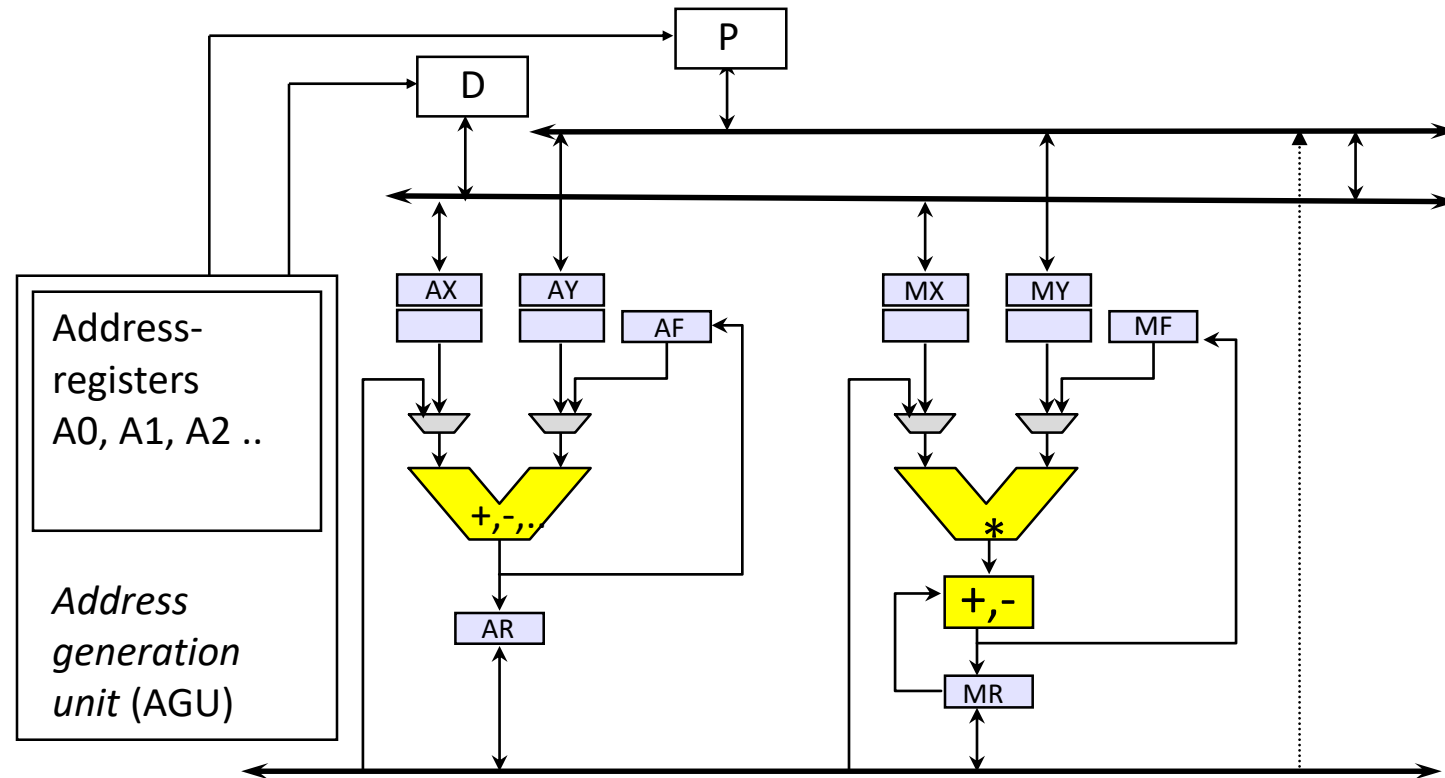
Example: Multimedia-Instructions

- Multimedia instructions exploit that many registers, adders etc. are quite wide (32/64 bit), whereas most multimedia data types are narrow (e.g. 8 bit per color, 16 bit per audio sample per channel).
- Idea: Several values can be stored per register and added in parallel.



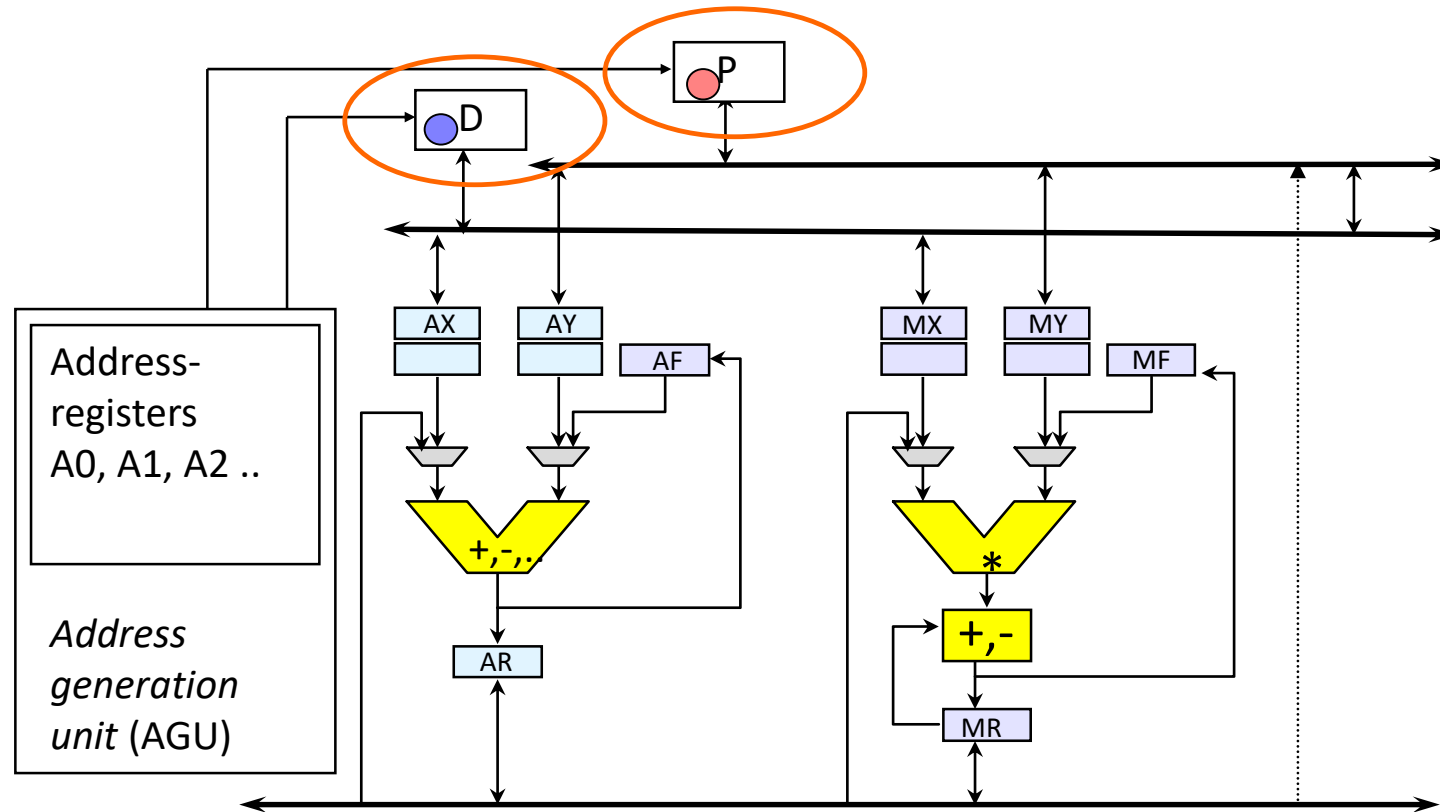
Example: Heterogeneous Processor Registers

Example (ADSP 210x):



Different functionality of registers AR, AX, AY, AF, MX, MY, MF, MR

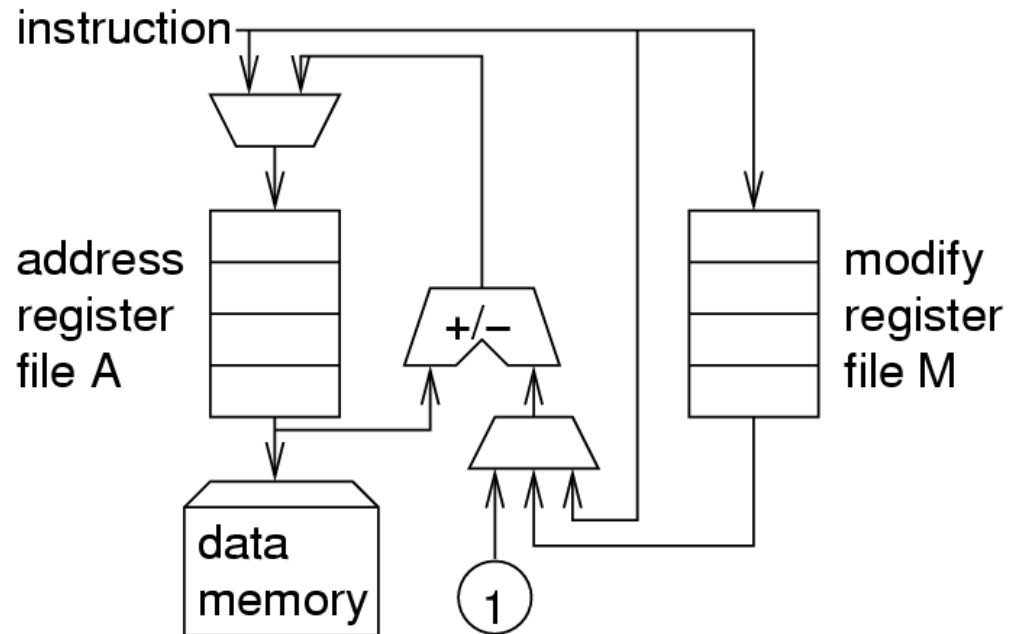
Example: Multiple Memory Banks



Enables parallel fetches for some operations

Example: Address Generation Units

Example (ADSP 210x):



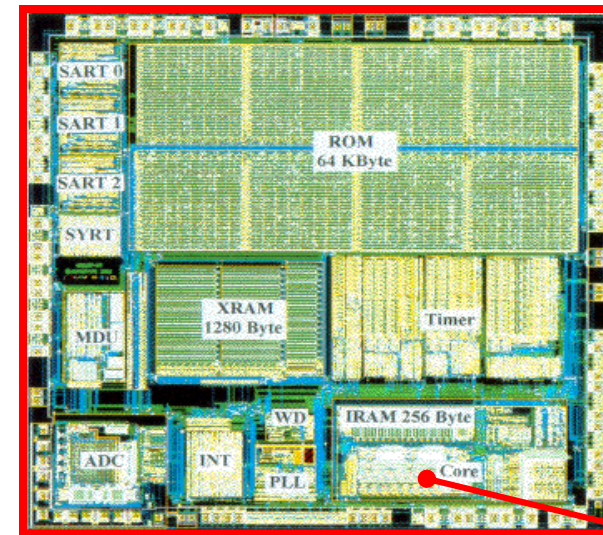
- Data memory can only be fetched with address contained in register file A, but its update can be done in parallel with operation in main data path (takes effectively 0 time).
- Register file A contains several precomputed addresses $A[i]$.
- There is another register file M that contains modification values $M[j]$.
- Possible updates:
 - $M[j] := \text{'immediate'}$
 - $A[i] := A[i] \pm M[j]$
 - $A[i] := A[i] \pm 1$
 - $A[i] := A[i] \pm \text{'immediate'}$
 - $A[i] := \text{'immediate'}$

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Microcontroller

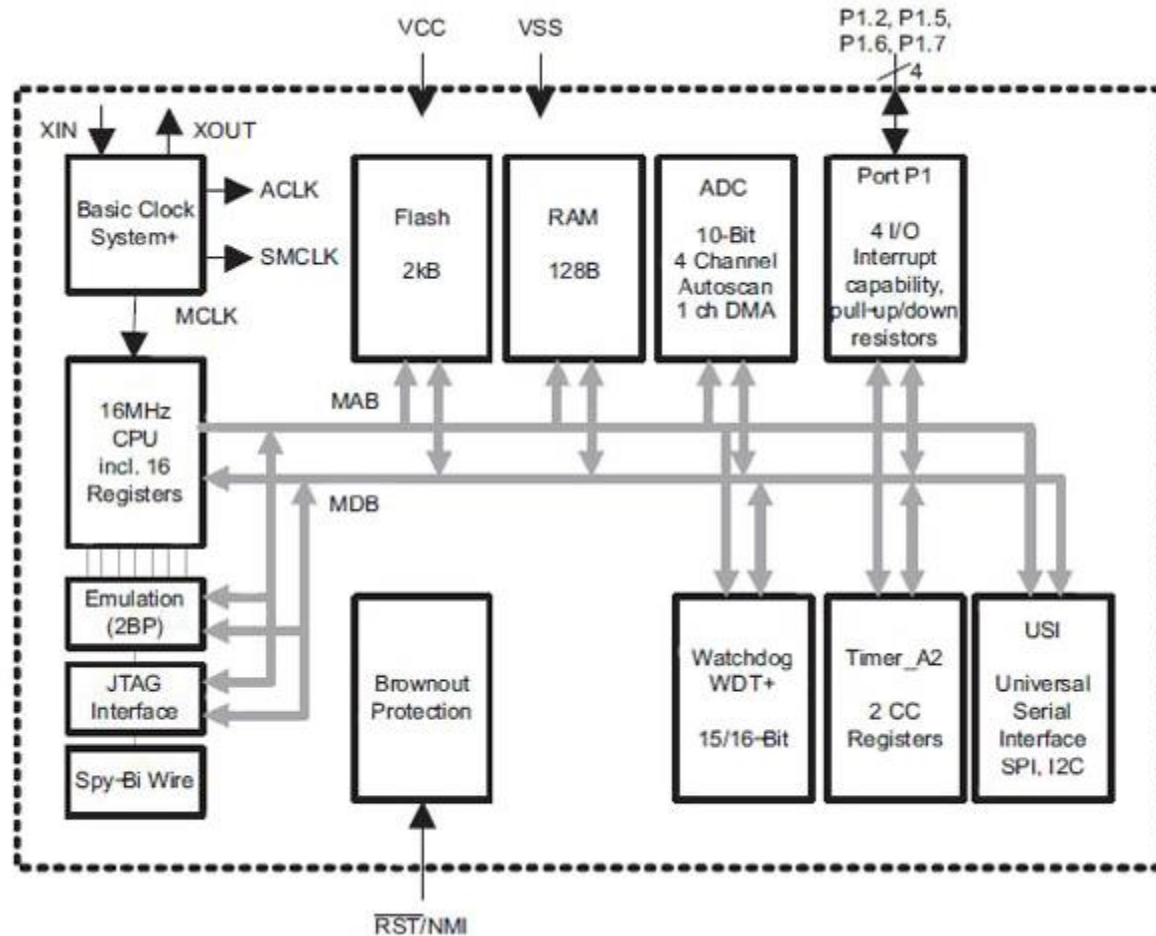
- *Control-dominant applications*
 - supports process scheduling and synchronization
 - preemption (interrupt), context switch
 - short latency times
- *Low power consumption*
- Peripheral units often integrated
- Suited for real-time applications



SIECO51 (Siemens)

8051 core

Microcontroller as a System-on-Chip



MSP 430 RISC Processor (Microchip)

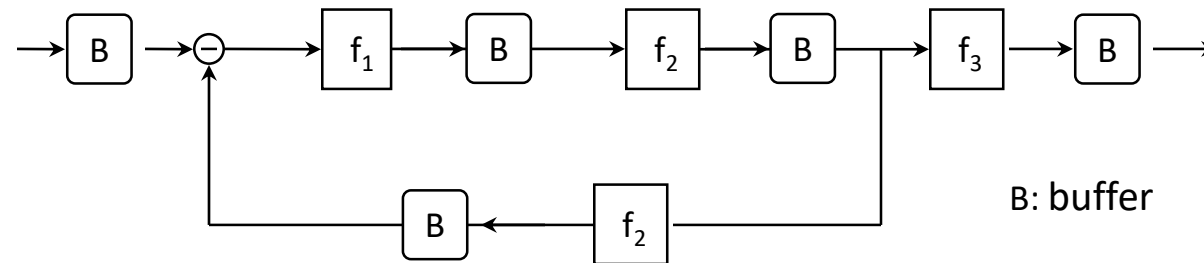
- complete system
- timers
- I²C-bus and par./ser. interfaces for communication
- A/D converter
- watchdog (SW activity timeout): safety
- on-chip memory (volatile/non-volatile)
- interrupt controller

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Data Dominated Systems

- *Streaming oriented systems* with mostly periodic behavior
- Underlying *model of computation* is often a signal flow graph or data flow graph:

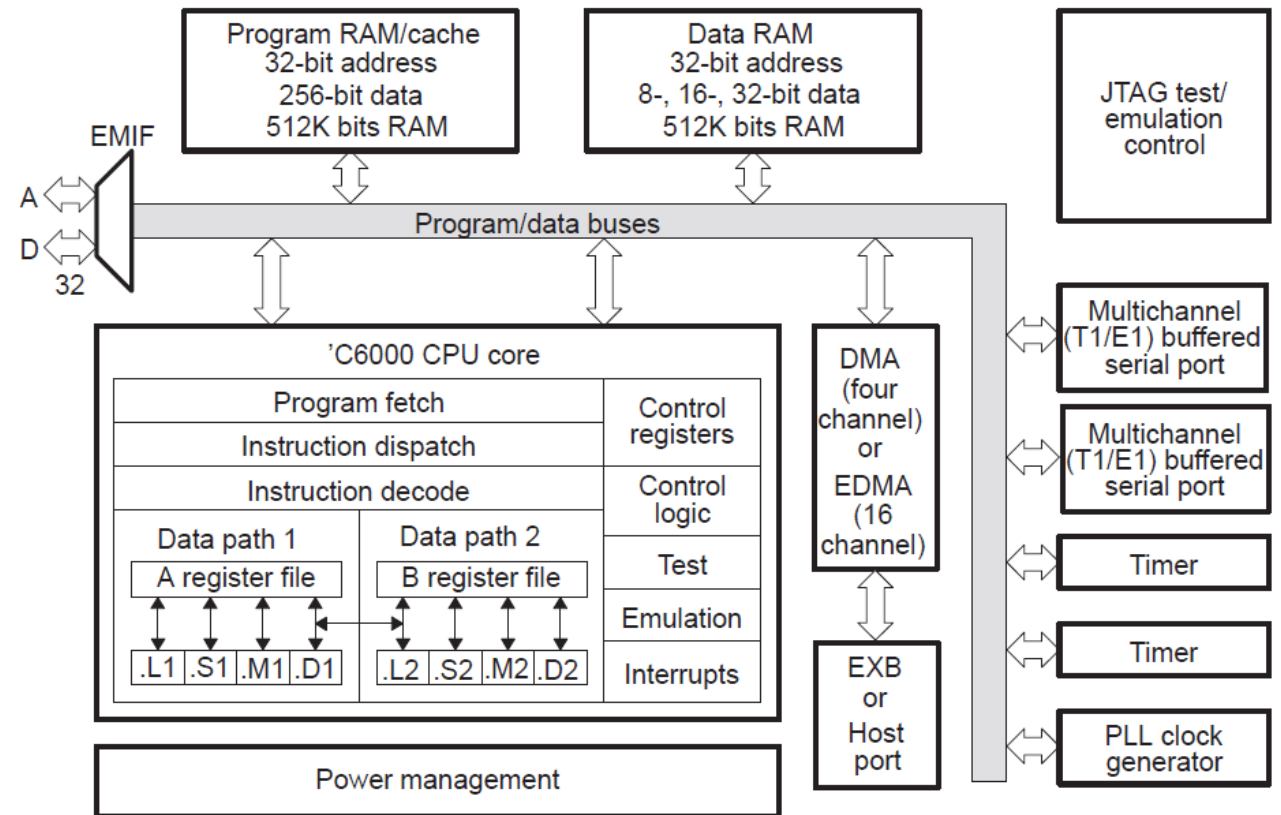


- Typical *application examples*:
 - signal processing
 - multimedia processing
 - automatic control

Digital Signal Processor

- *optimized for data-flow applications*
- suited for simple control flow
- parallel hardware units (VLIW)
- specialized instruction set
- high data throughput
- zero-overhead loops
- specialized memory
- *suited for real-time applications*

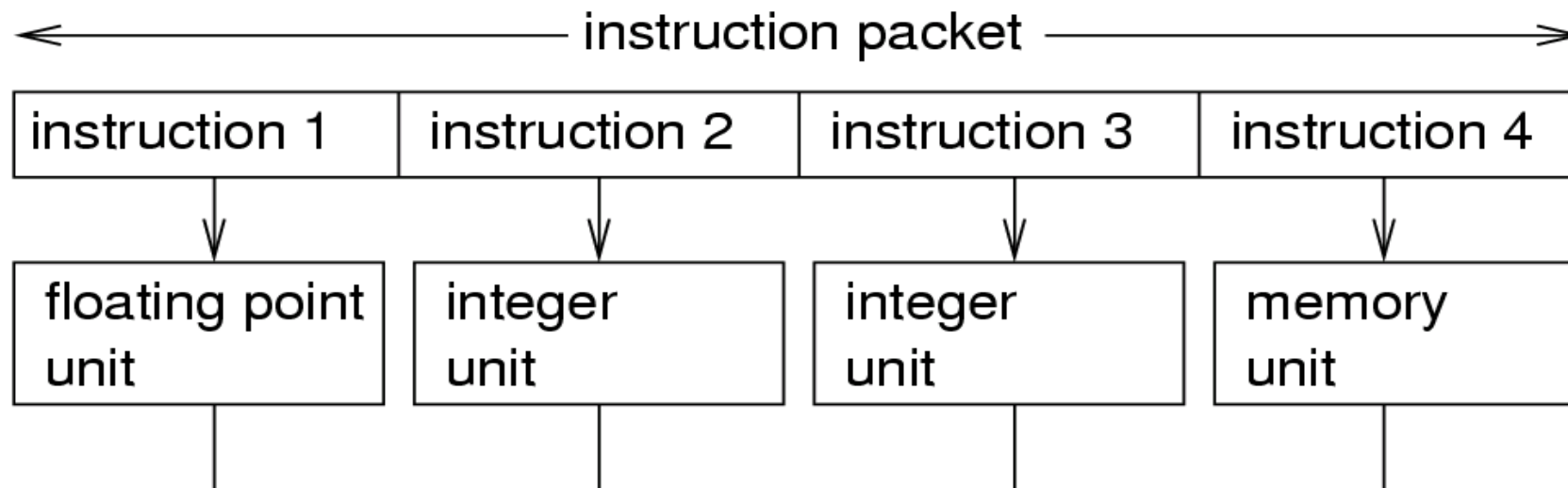
Figure 2–1. TMS320C62x/C67x Block Diagram



Very Long Instruction Word (VLIW)

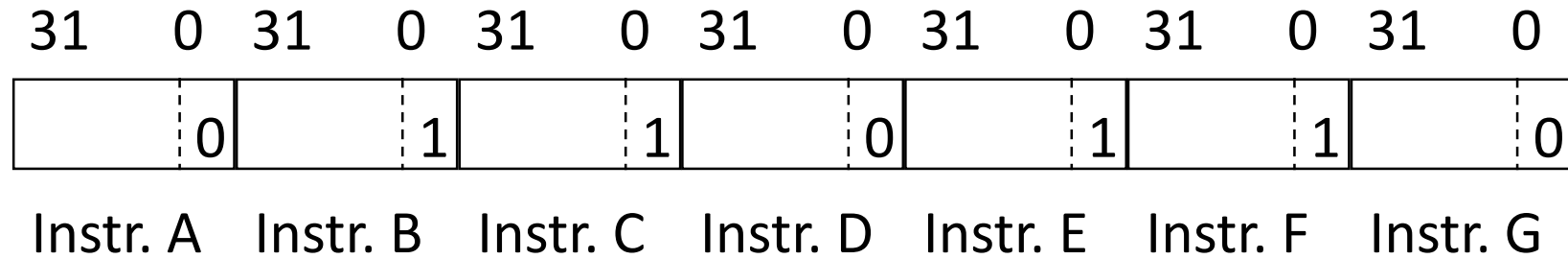
Key idea: detection of possible parallelism to be done by compiler, not by hardware at run-time (inefficient).

VLIW: parallel operations (instructions) encoded in one long word (instruction packet), each instruction controlling one functional unit.



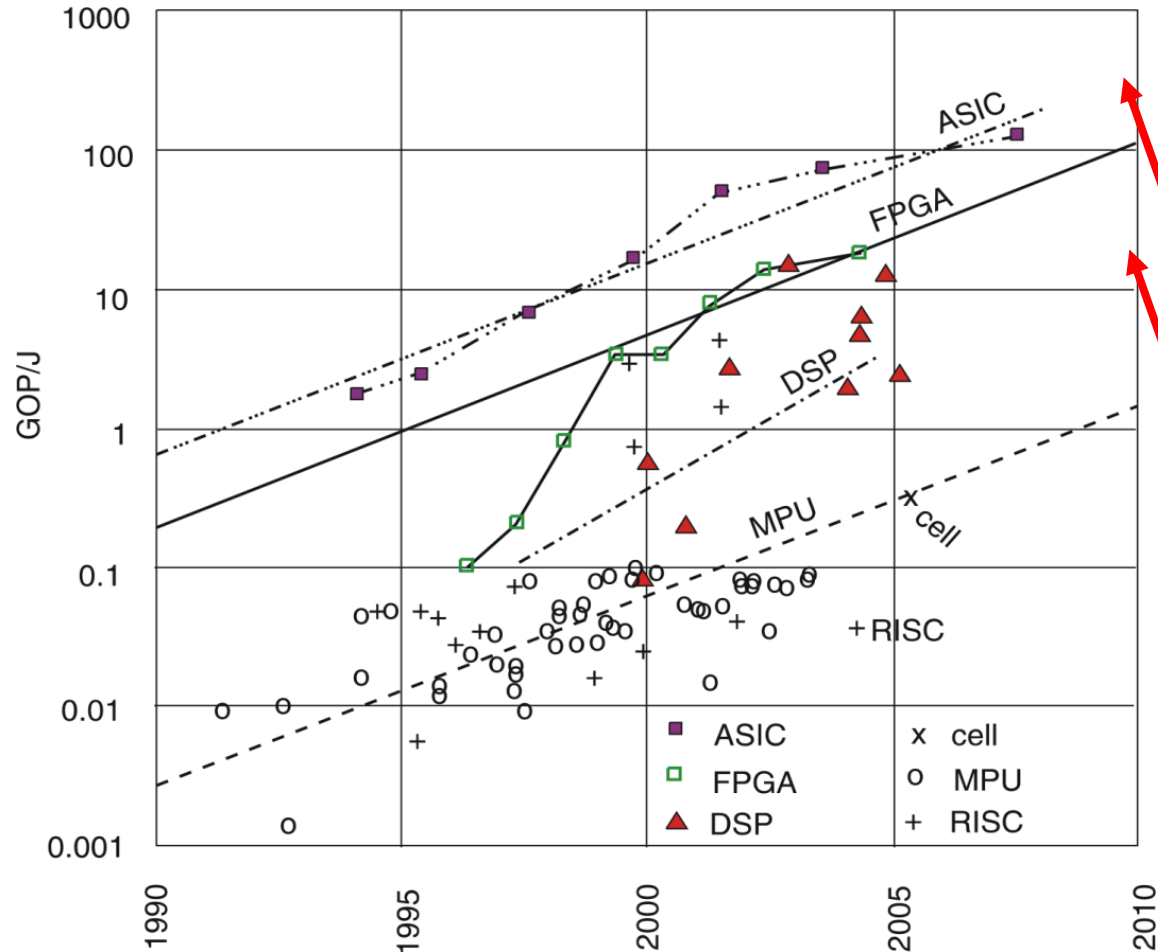
Explicit Parallelism Instruction Computers (EPIC)

The TMS320C62xx VLIW Processor as an example of EPIC:

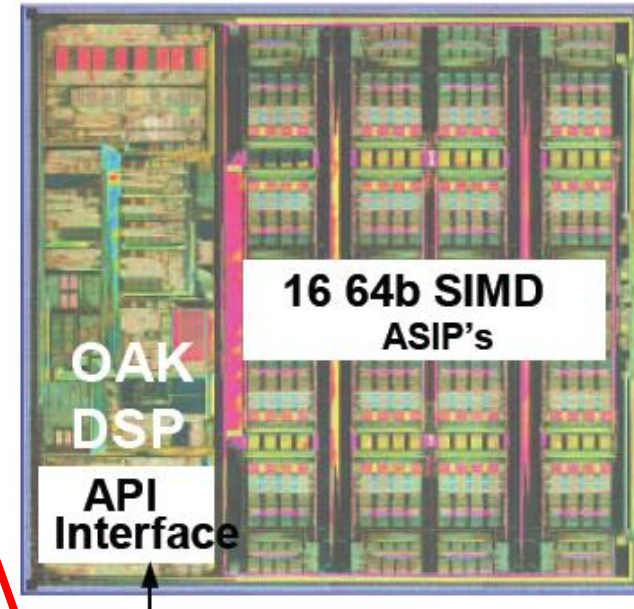


| Cycle | Instruction |
|-------|-------------|
| 1 | A |
| 2 | B C D |
| 3 | E F G |

Example Infineon

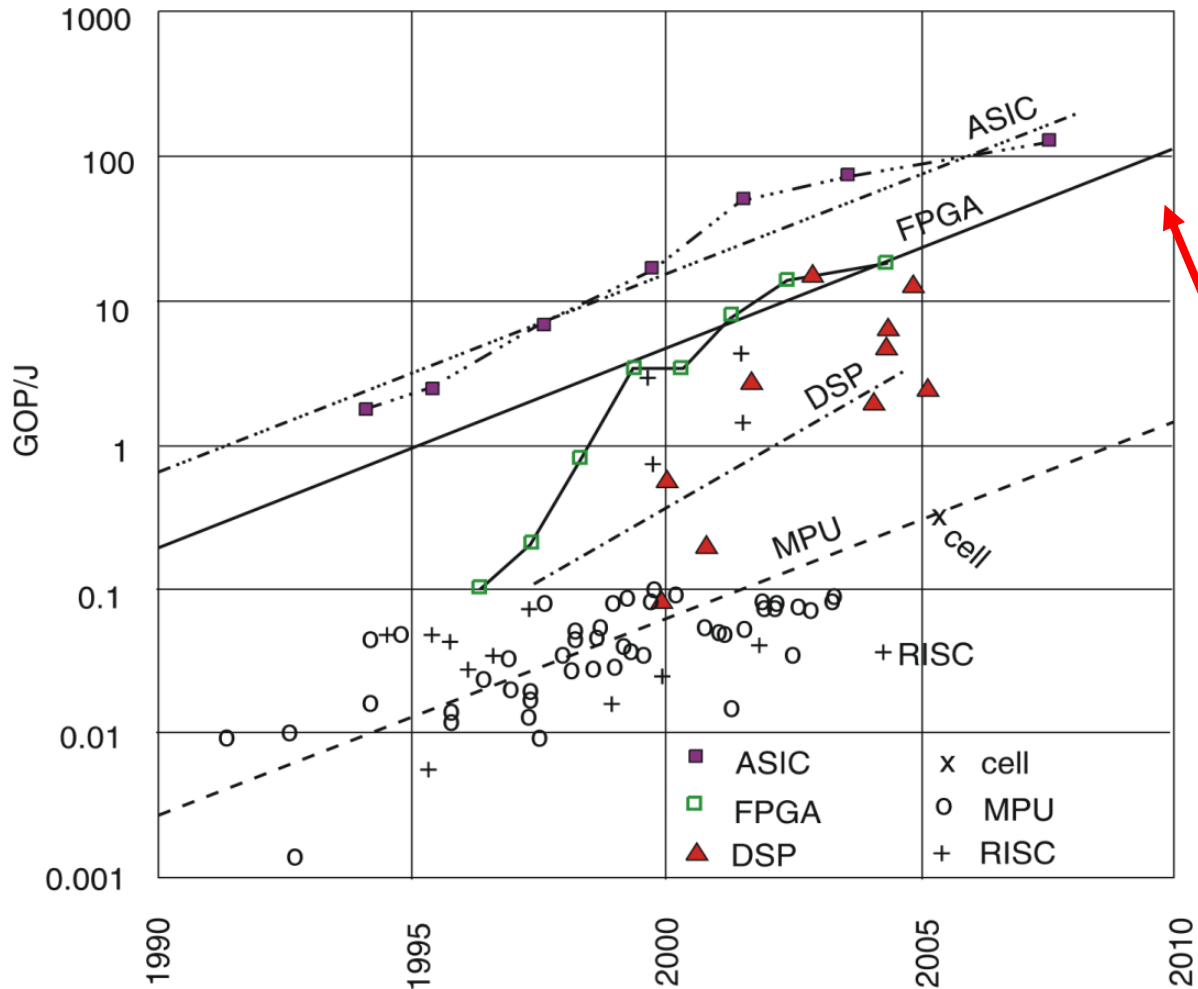


Processor core for car mirrors
Infineon

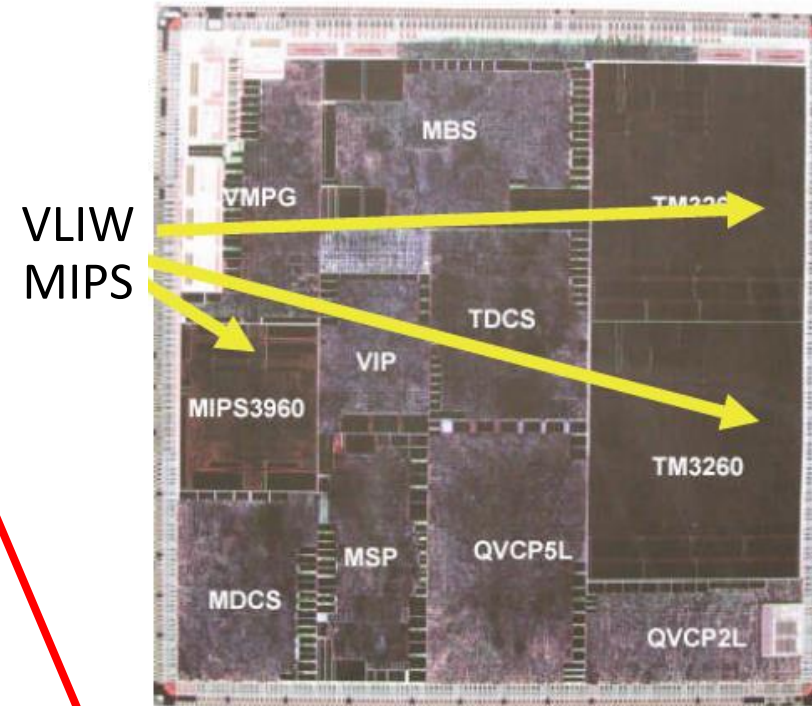


200MHz , 0.76 Watt
100Gops @ 8b
25Gops @ 32b

Example NXP Trimedia VLIW



Nexperia Digital Video Platform NXP



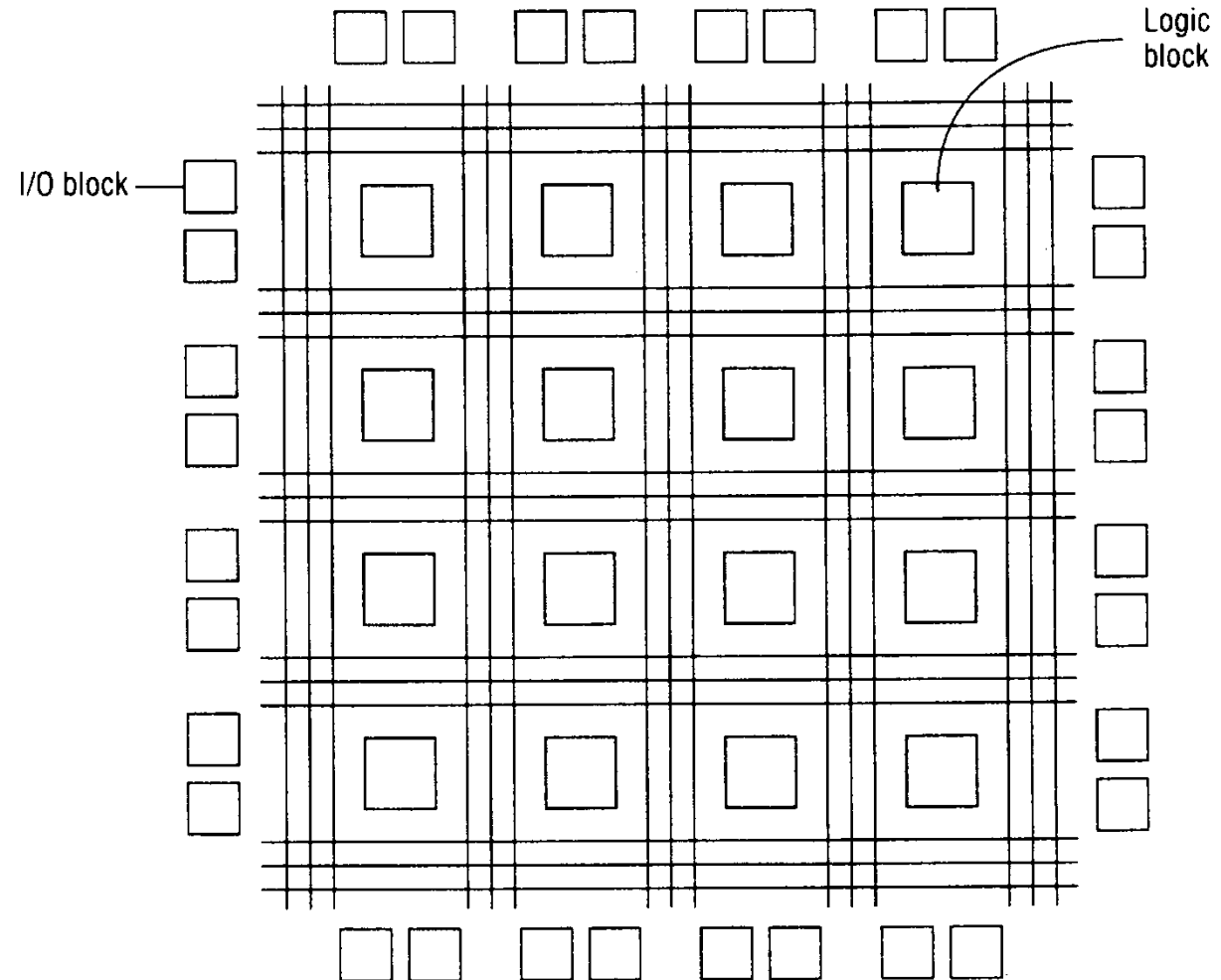
**1 MIPS, 2 Trimedia
60 coproc,
266MHz, 1.5 watt 100 Gops**

Topics

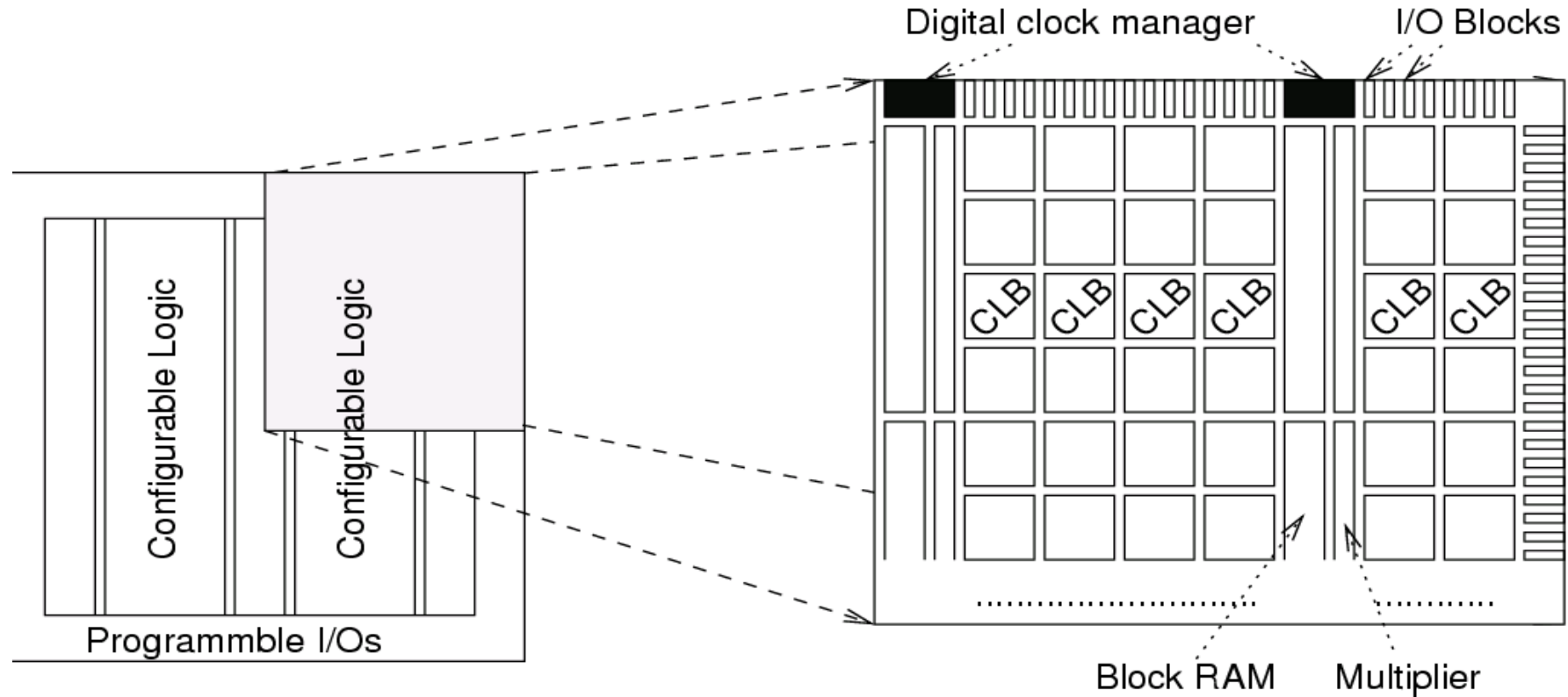
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FPGA – Basic Structure

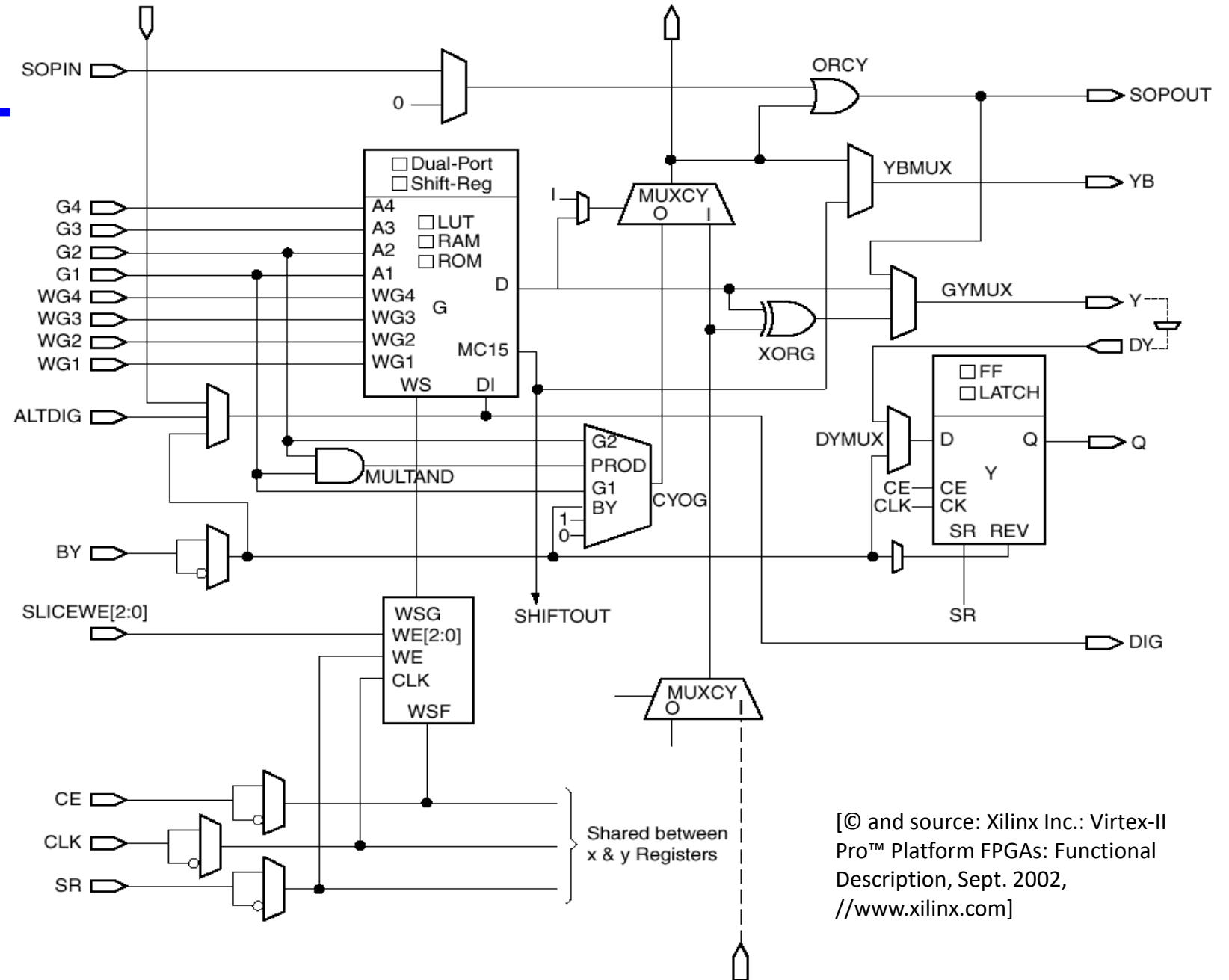
- Logic Units
- I/O Units
- Connections



Floor-plan of VIRTEX II FPGAs



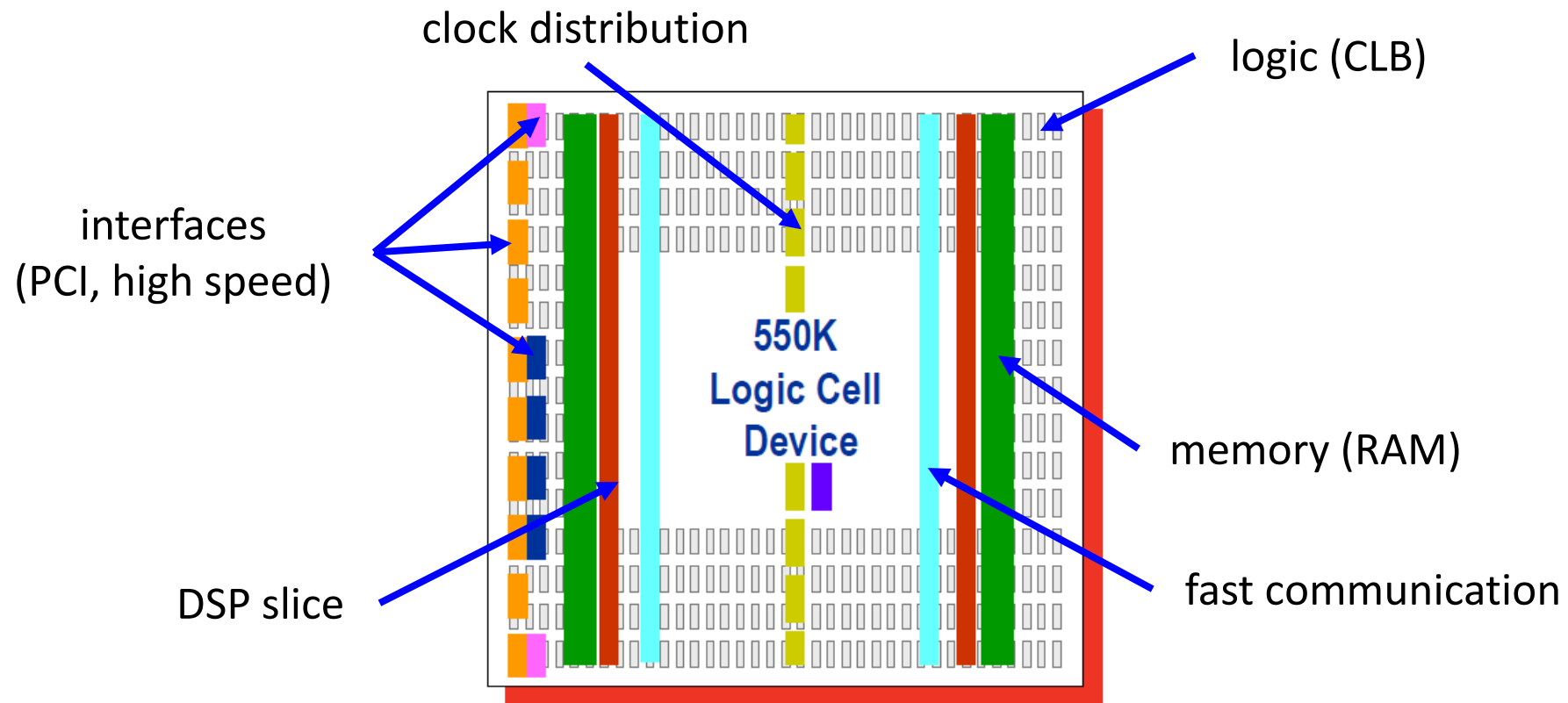
Virtex Logic Cell



[© and source: Xilinx Inc.: Virtex-II Pro™ Platform FPGAs: Functional Description, Sept. 2002, //www.xilinx.com]

Example Virtex-6

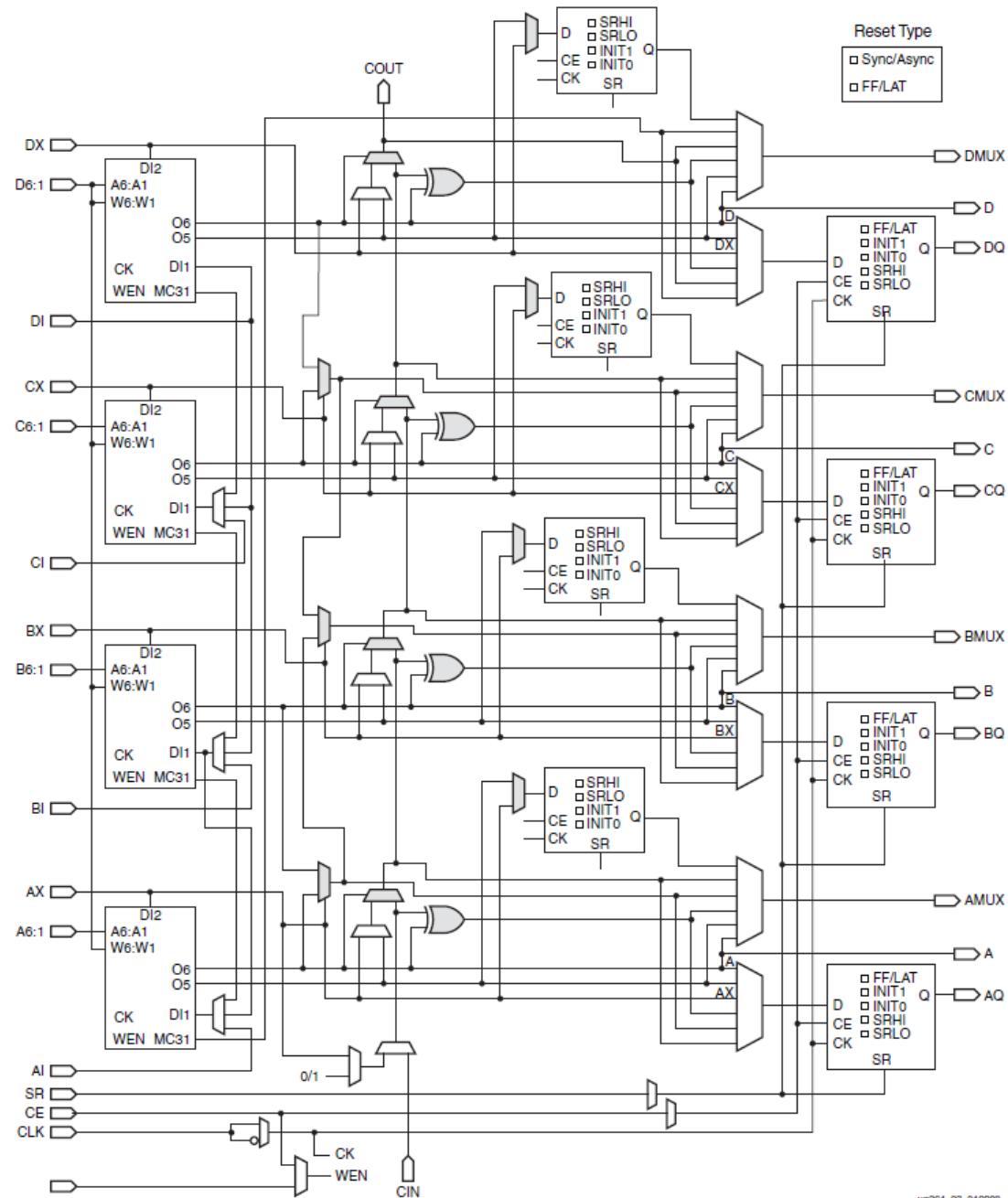
- Combination of flexibility (CLB's), Integration and performance (heterogeneity of hard-IP Blocks)



XILINX Virtex UltraScale

| | |
|-------------------|--------|
| Effective LEs (K) | 3,435 |
| Logic Cells (K) | 2,863 |
| UltraRAM (Mb) | 432.0 |
| Block RAM (Mb) | 94.5 |
| DSP Slices | 11,904 |
| I/O Pins | 832 |

Virtex-6 CLB Slice



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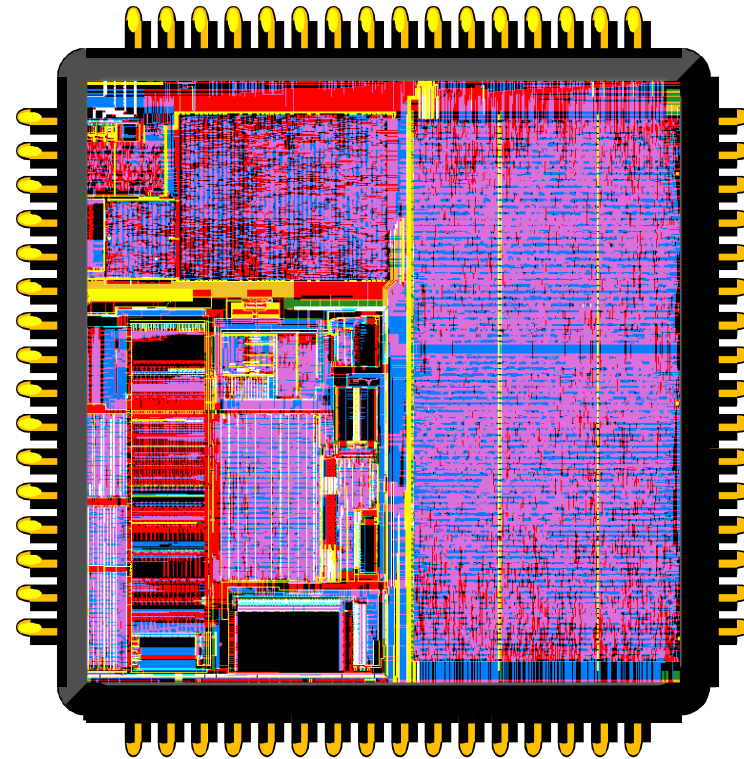
Application Specific Circuits (ASICs)

Custom-designed circuits are necessary

- if ultimate speed or
- energy efficiency is the goal and
- large numbers can be sold.

Approach *suffers* from

- long design times,
- lack of flexibility
(changing standards) and
- high costs
(e.g. Mill. \$ mask costs).



Topics

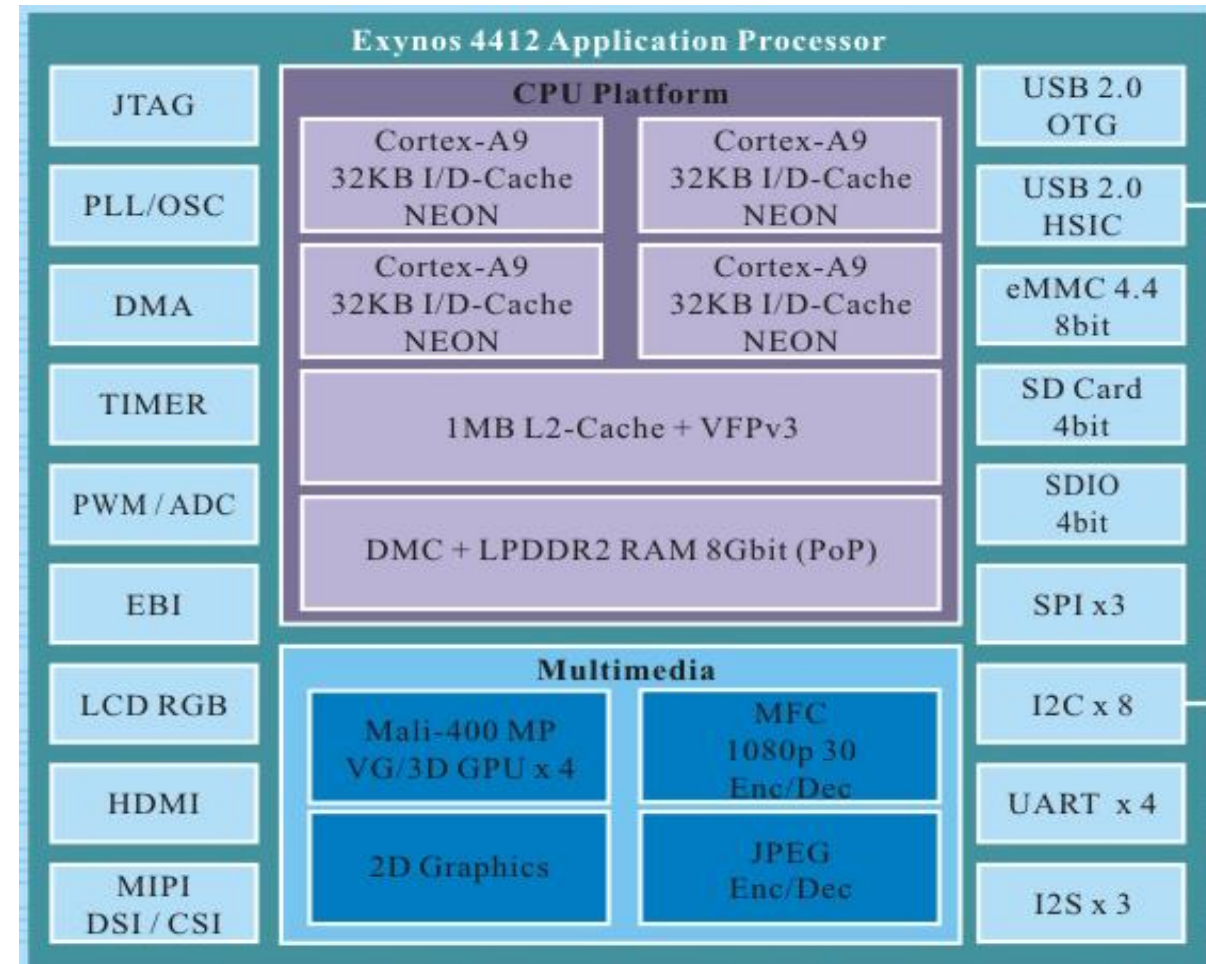
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- **Heterogeneous Architectures**

Example: Heterogeneous Architecture



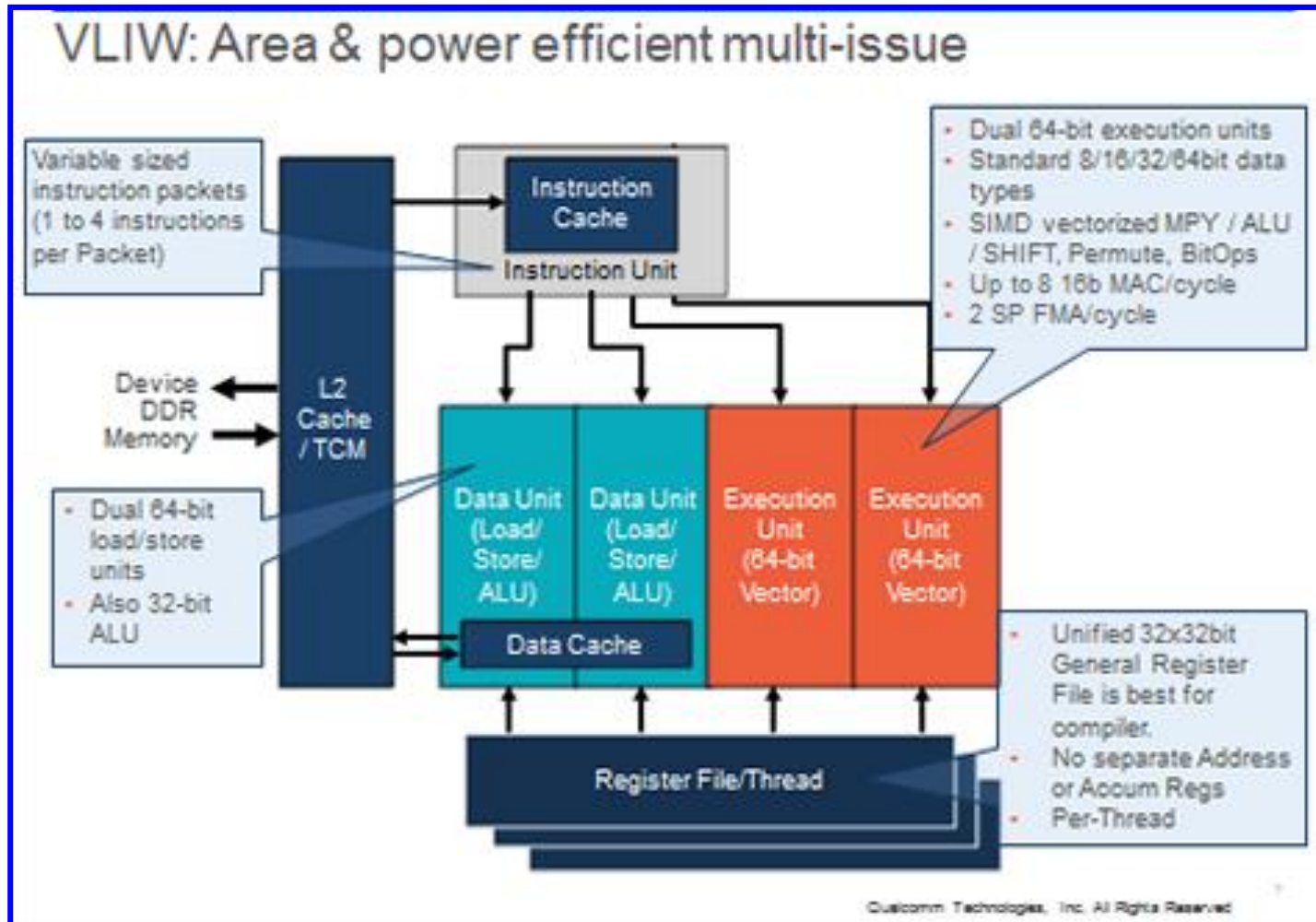
Samsung Galaxy Note II

- Exynos 4412 System on a Chip (SoC)
- ARM Cortex-A9 processing core
- 32 nanometer: transistor gate width
- Four processing cores



Example: Heterogeneous Architecture

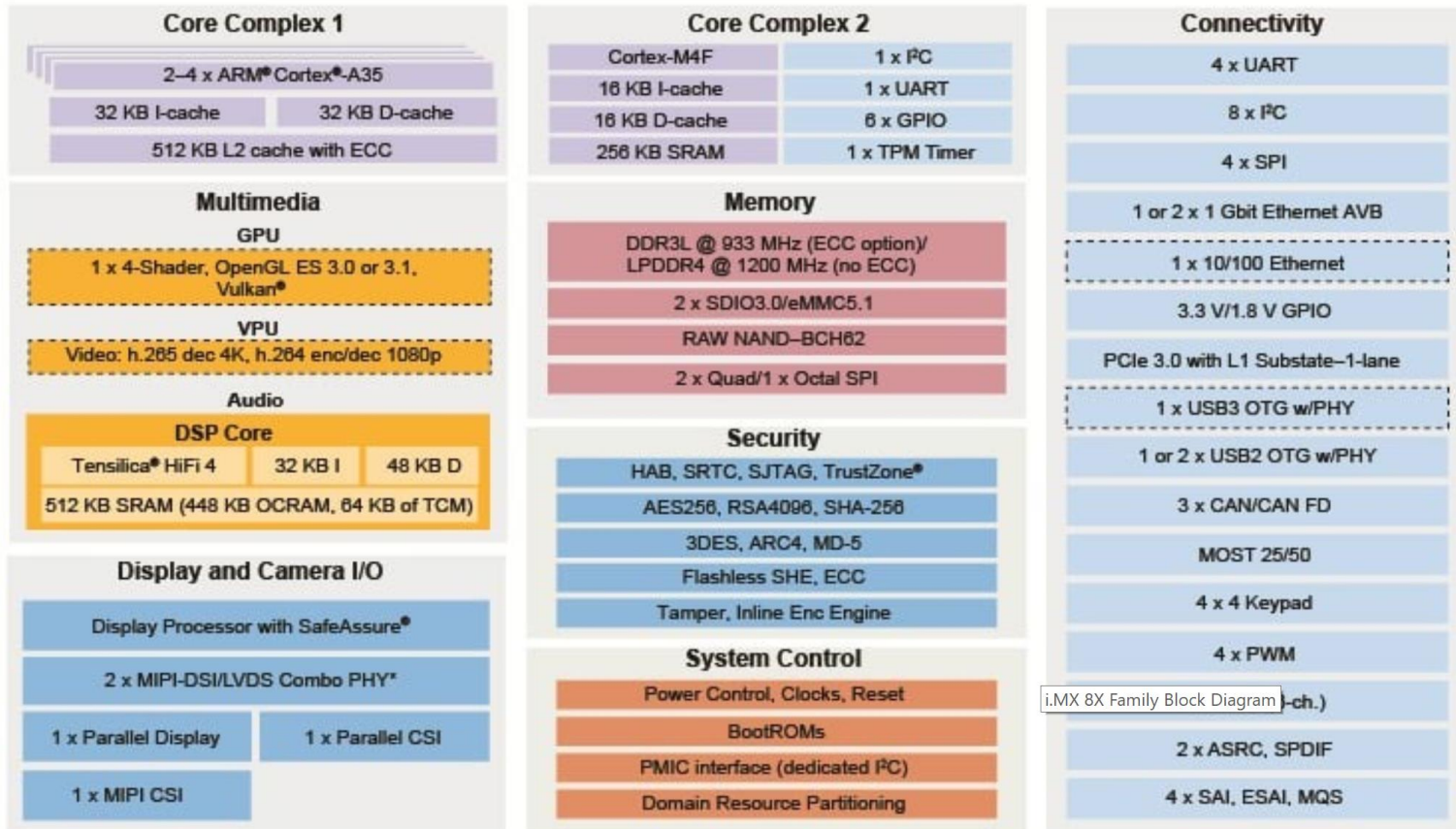
Hexagon DSP



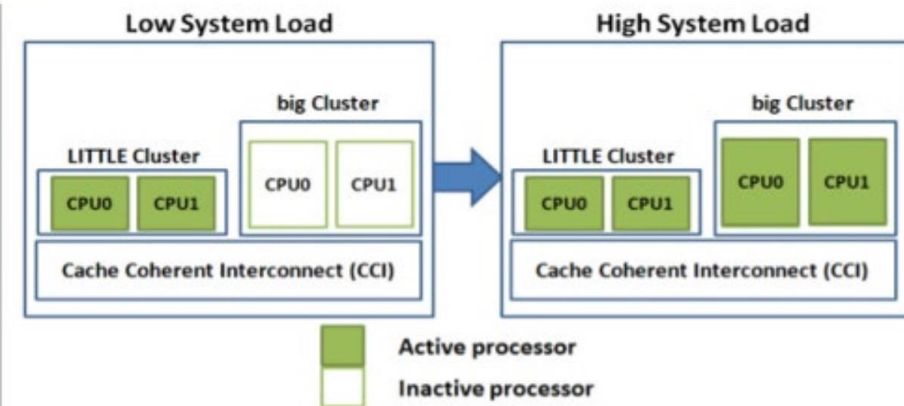
Snapdragon 835 (Galaxy S8)



Example: ARM big.LITTLE Architecture



Toradex Colibri Compute-on-Module



Available on certain product families Note: Accessing muxable controller's full capabilities is dependent upon board component choice