Low-Power System Design

227-0781-00L

Fall Semester 2019

Jan Beutel

Plan for Today

- Recap logistics if anyone is new
  - Lecture
  - Reading/Writing Seminar
  - Hands-on Design Project

- Evolution of low-power embedded sensing systems
- LP system architectures – processor systems
- Application example
  - PermaSense Project Architecture

Low-Power System Design

COURSE LOGISTICS

Course Components

- Goals of LPSD
  - Introduction to the state-of-the-art in research
  - Empowering students to ask relevant questions and develop ideas critically
  - Enable students to work on a research project of publishable quality

- Components
  - Up front lecture with slides (please make it interactive, ask questions)
  - Reading and writing seminar
  - Hands-on practical work, design project

Course Resources

- Online course web page
  https://www.tec.ee.ethz.ch/education/lectures/low-power-system-design.html
  - Syllabus
  - Reading material
  - Assignments
  - Links to further resources
  - Updates to material as we progress
- Riot chat room for reading seminar: #lpsd:matrix.ee.ethz.ch
  - Submitting reviews
  - Discussion
  - Sharing of other related papers, interesting stuff
  - Questions/Answers
- In case of questions: janbeutel@ethz.ch

Lecture Schedule

Week	Date	Lecture Wednesday 10-12h	Lab Exercises Wednesday 13-15h
1	18.09.2019	Lecture 1 - Course Introduction, Definitions, Metrics	Reading/Writing Seminar Introduction
2	25.09.2019	Lecture 2 - LP System Architectures	Lab 1
3	02.10.2019	Lecture 3 – LP System Architectures	Lab 2
4	09.10.2019	**No Lecture - Reading Seminar only**	Lab 3
5	16.10.2019	**No Lecture - Reading Seminar only**	Lab 4
6	23.10.2019	Lecture 4 – Networked Embedded Systems	Intro Design Project
7	30.10.2019	Lecture 5 – Networked Embedded Systems	Technical Support for Design Project
8	06.11.2019	Lecture 6 – Networked Embedded Systems	Technical Support for Design Project
9	13.11.2019	Lecture 7 - Networked Embedded Systems	Technical Support for Design Project
10	20.11.2019	Lecture 8 - Modeling, Tools and Methods for Power Analysis	Technical Support for Design Project
11	27.11.2019	Lecture 9 - Modeling, Tools and Methods for Power Analysis	Technical Support for Design Project
12	04.12.2019	Lecture 10 - Renewable Energy	Technical Support for Design Project
13	11.12.2019	Lecture 11 - Renewable Energy	Technical Support for Design Project
14	18.12.2019	Lecture 12 - Project Presentations	Student Presentations of Design Project

Daily Synopsis

- Lecture (~60-75 min)
  - Recap last lecture, introduce structure of topics & objective of today's lecture
  - Daily lecture
  - Feed in a daily
    - Hot research topic/paper of the day
    - Prominent research figure in the area
    - Practical example (success story or failure)
  - Recap objective of the day

- Reading and Writing Seminar (~30 min)
  - Short presentation by group of students
  - Discussion of papers
  - Introduce reading for next week

- Exercises, Lab and Reading Time (2x 45 min)
  - Dual Processor Platform (DPP) on loan for everyone
  - Introduction to DPP platform & FlockLab testbed
  - DPP tutorial support
  - Small design project in groups of 2-3 over whole length of the course

Reading and Writing Seminar

- Reading assignment of 1 paper per week – **until FRIDAY**
  - 2-3 students prepare a written summary (max. 200-300 words)
    - Write-up should contain the (i) essential points of the paper, (ii) it's main contribution and (iii) your assessment
    - Research of related work: recent papers, different approaches, historical background…
  - Summary is shared with all via discussion forum (matrix chatroom)

- Discussion/questions/comments – **FRIDAY to WEDNESDAY**
  - EVERYBODY comments on review summary and paper
    - Your own opinion
    - Corrections/additions to the reviewers voice
    - Additional questions
  - Joint search for related work, interesting ecosystem etc.

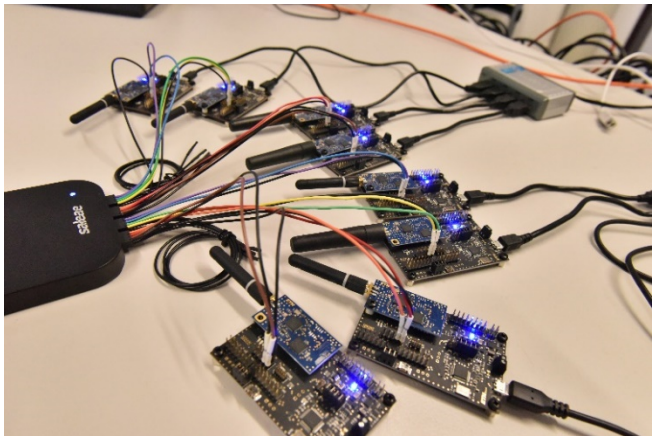
- Joint discussion of papers in class – **WEDNESDAY in class**
  - Short presentation of paper and summary in class to kick off discussion
  - Presentation using max. 3-4 slides (not a full paper presentation)

- Reading/writing and your contributing to the discussions is part of the grade (30%)

- Assignment via signup sheet with
  - 1x summary write-up/paper presentation
  - 4x review/commenting per student

Hands-on Practical Design Project

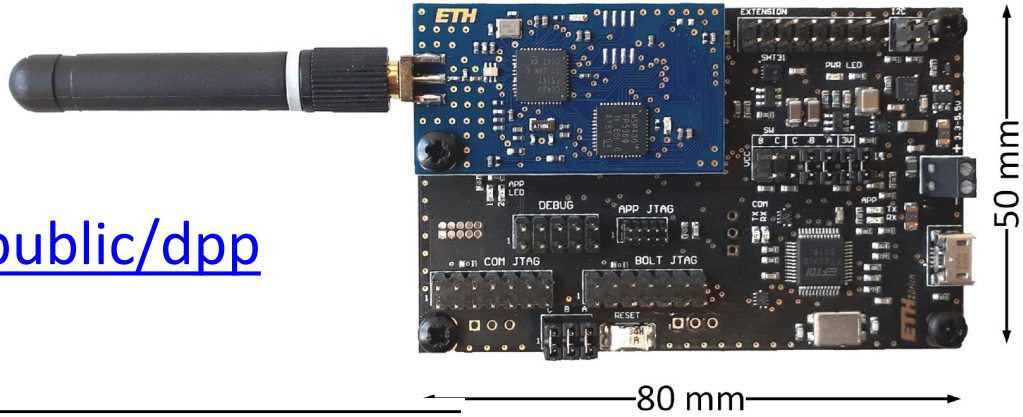
- Design project using Dual Processor Platform (DPP)



- In groups (of 2-3) develop a low-power application
  - Introduction to state-of-the-art tools
  - Effective power consumption effects should be visible
  - Focus on aspects of dynamic range
- Presentation and discussion of results in final lecture
- Tournament: Best team is awarded a prize

Resources for Hands-on

- Dual-Processor Platform
  - State-of-the-Art Sensor network platform
  - ETH-built…



https://gitlab.ethz.ch/tec/public/dpp

DPP2 SX1262 ComBoard
ST STM32L433CC, 256k ROM, 64k SRAM, 80 MHz
RAM2 (16 KiB) has option for retention
0.28 µA (standby with RTC), 7 µs wakeup from stop mode
−148 dB at (SF12, 125 kHz), 389 mW at +22 dB m
LoRa, GFSK

Resources for Hands-on

Arm® Cortex®-M4 (DSP + FPU) – 80 MHz

- ART Accelerator™
- USART, SPI, I²C
- Quad-SPI
- 16- and 32-bit timers
- SAI + audio PLL
- SWP
- 2x CAN
- 2x 12-bit DACs
- Temperature sensor
- Low voltage 1.71 to 3.6 V
- V_{BAT} mode
- Unique ID
- Capacitive touch sensing
- AES-128/256* and SHA-256**

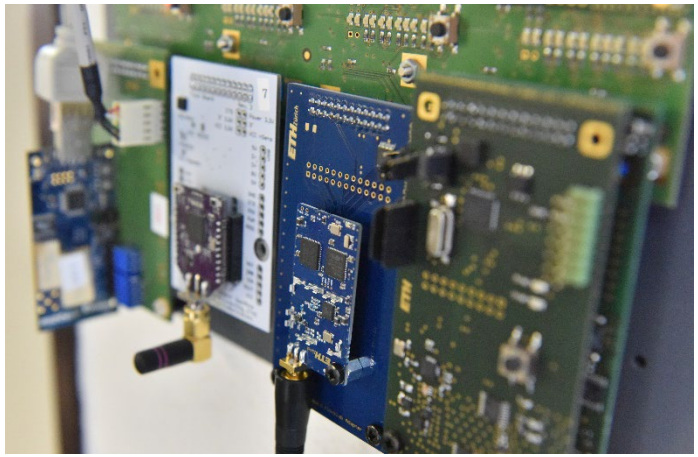
STM32 L4 Product line	Flash (KB)	RAM (KB)	Memory I/F FSMC	Op-Amp	CAN	Sigma Delta Interface	12-bit ADC 5 Msps 16-bit HW oversampling	DAC	SAI	USB2.0 OTG FS	USB Device	Segment LCD driver	Chrom-ART Accelerator™
STM32L4x6 - USB OTG + Segment LCD Lines													
STM32L496**	512 to 1024	320	•	2	2	8x ch	3	2	2	•		Up to 8x40	•
STM32L476*	256 to 1024	128	•	2	1	8x ch	3	2	2	•		Up to 8x40	
STM32L4x5 - USB OTG lines													
STM32L475	256 to 1024	128	•	2	1	8x ch	3	2	2	•			
STM32L4x3 - USB Device + Segment LCD lines													
STM32L433*	128 to 256	64		1	1		1	2	1		•	Up to 8x40	
STM32L4x2 - USB Device lines													
STM32L452*	256 to 512	160		1	1	4x ch	1	1	1		•		
STM32L432*	128 to 256	64		1	1		1	2	1		•		
STM32L412*	64 to 128	40		1			2				•		
STM32L4x1 - Access lines													
STM32L471	512 to 1024	128	•	2	1	8x ch	3	2	2				
STM32L451	256 to 512	160		1	1	4x ch	1	1	1				
STM32L431	128 to 256	64		1	1		1	2	1				

Note: * HW crypto/hash functions are available on STM32L486, STM32L443, STM32L462, STM32L442 and STM32L422 - ** on STM32L4A6

Resources for Hands-on

- DPP dev-board on loan for everyone for duration of semester
- FlockLab Testbed
  - Testbed of 30+ nodes
  - Remote programming of nodes
  - Testing of applications in larger networks
  - Power profiling, digital tracing/actuation
- FlockLab is a shared/limited resource
  - Only one user active per time slice
  - Need to accommodate everyone
- Cooja Simulator support
- Support through online forums and TA's
  - Roman Trueb roman.trueb@tik.ee.ethz.ch
  - Matthias Meyer matthias.meyer@tik.ee.ethz.ch
  - Reto Da Forno reto.daforno@tik.ee.ethz.ch

FlockLab



http://www.flocklab.ethz.ch/

Grading

- Official announcement
  - 30% contributions to the reading/writing seminar
  - 70% oral exam
- Hands-on design project
  - A successful design project will count positive towards the oral exam grade
  - Part of the oral exam will review your proposed solution and the concepts underlying the implementation

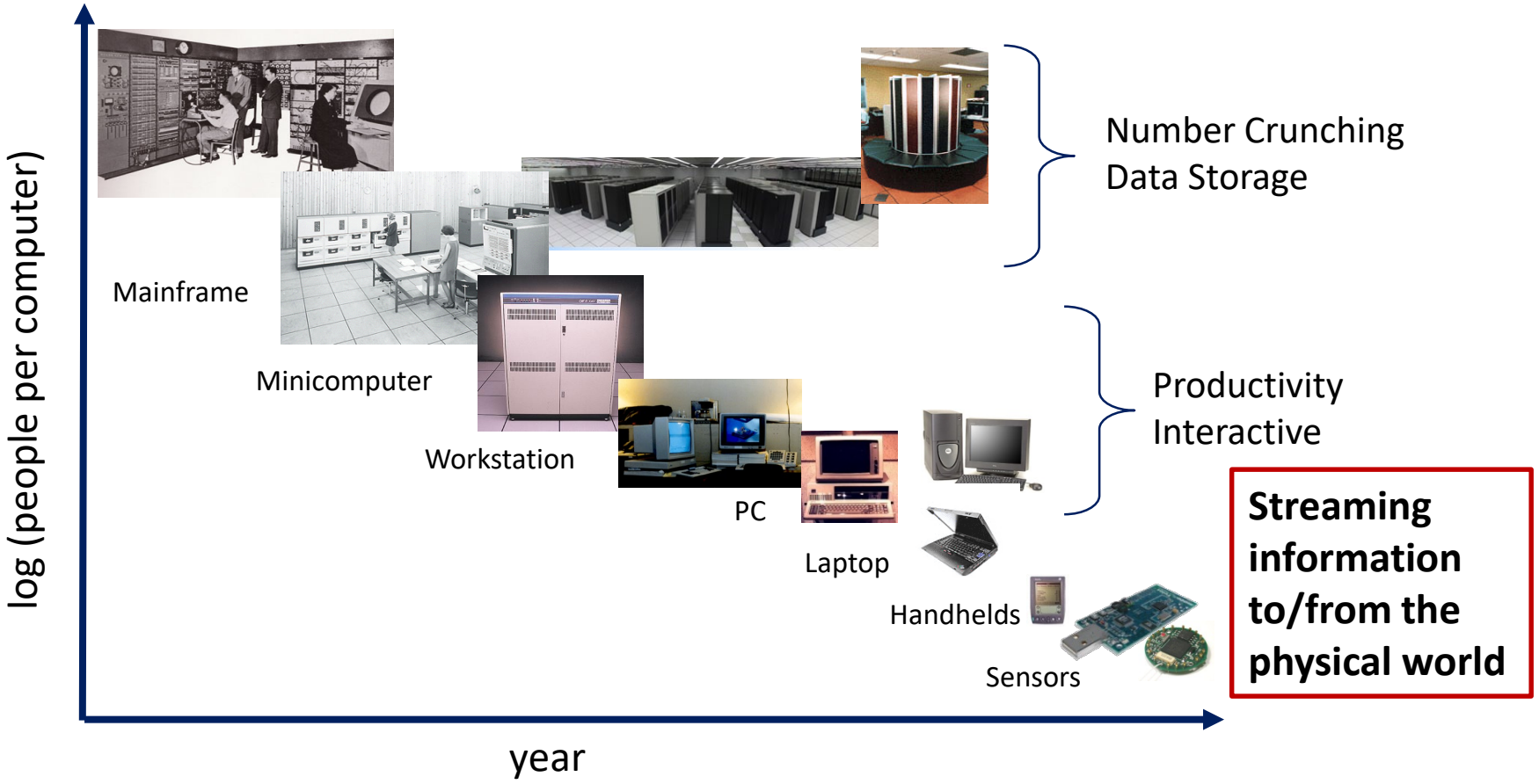
Some Comments

- Course will mean quite some work for you.
- Reading takes some time. Use Wednesday afternoons.
- Will shift around timing as needed.
- Also we can discuss your topics/questions as needed.
- Hands-on design project was very successful in past years
  - Depends on your own laptop infrastructure
  - Need to share resources on FlockLab testbed
  - Requires you to plan ahead (not just a last minute effort)

Low-Power System Design

LOW-POWER EMBEDDED SENSING SYSTEMS

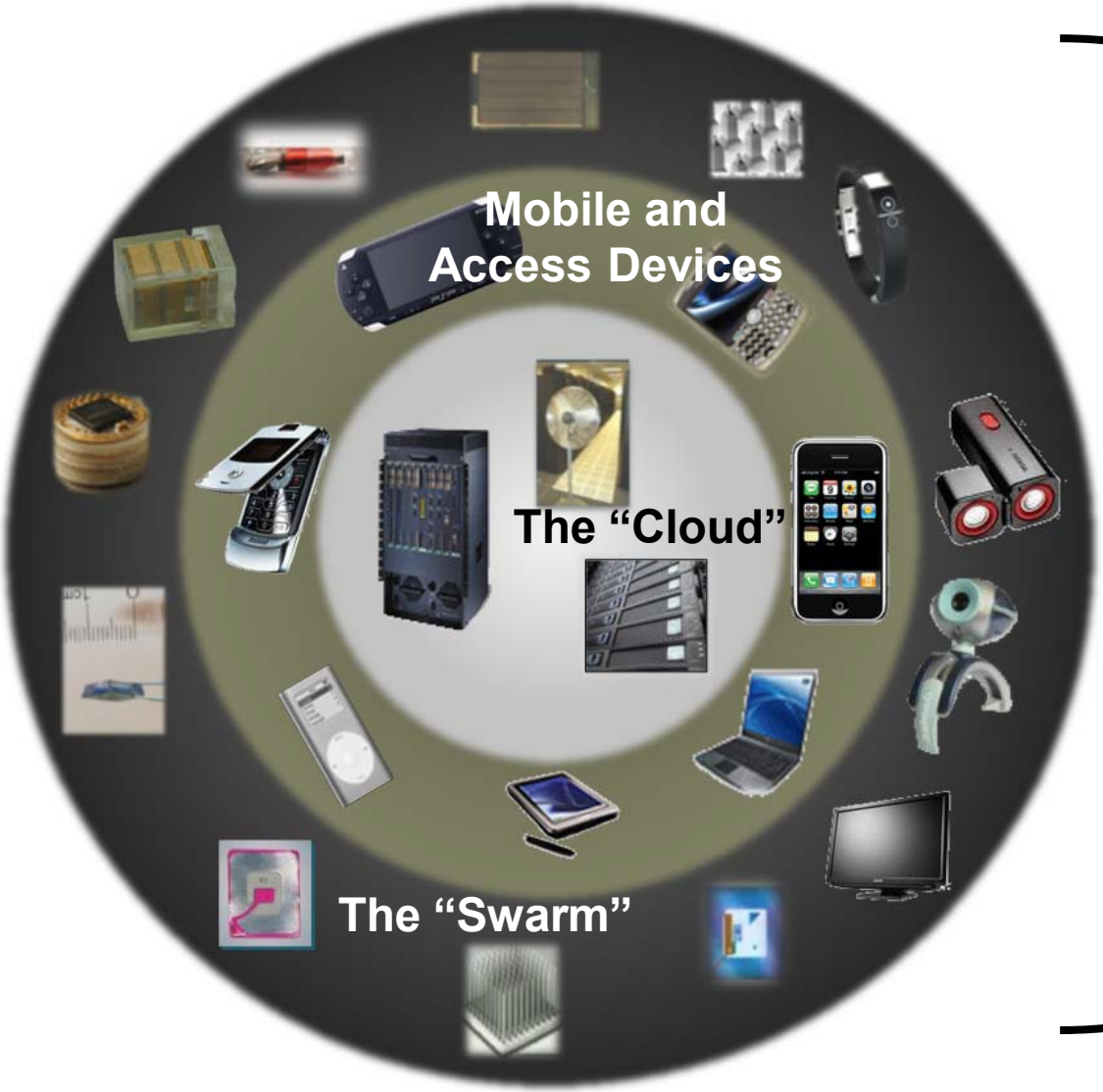
Bell's Law: New class of Computers Emerges Every 10 Years



Ever cheaper, ever smaller, ever more networked…

Figure abridged from D. Culler

The Network is the System



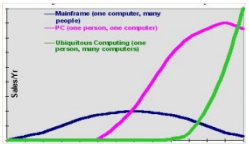
Power is an issue at all system levels and scales

Figure abridged from Jan Rabaey, UCB

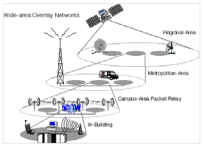
Wireless Sensor Networks

Visions 1991 1996 1999 2000 2001 2003 2004

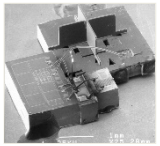
Ubiquitous Vision



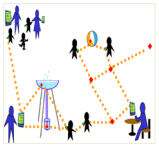
Wireless Overlay



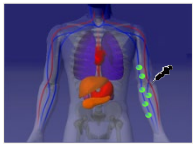
Smart Dust



PicoRadio

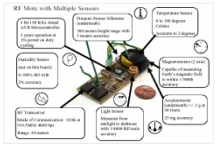


Directed Diffusion

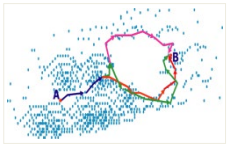


Paintable Computing

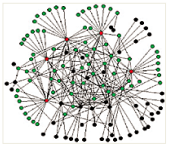
COTS Dust



Terminodes



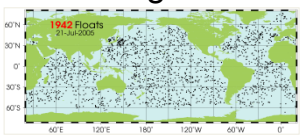
Scale Free Networks



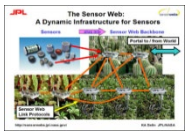
Applications 2000 2001 2003 2004

.....

Argo

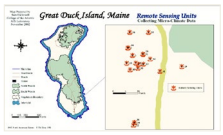


Sensor Webs



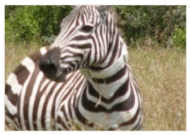
Military Surveillance

Duck Island

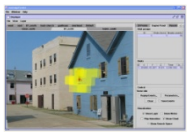


James Reserve

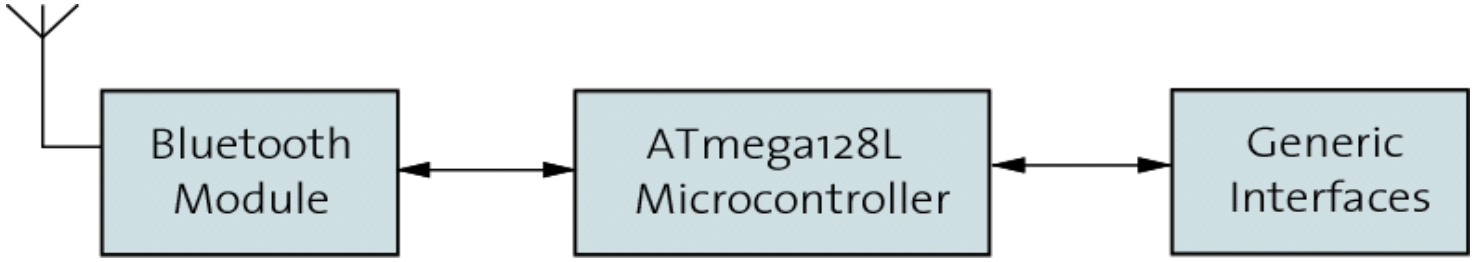
ZebraNet

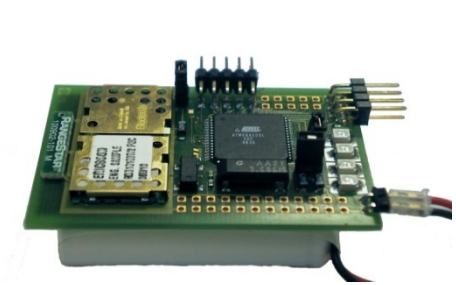


Shooter Localization

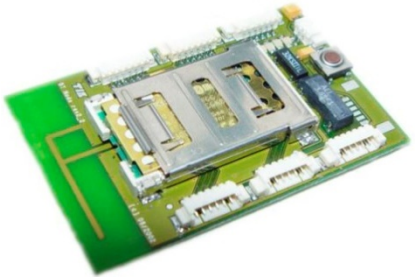


Typical Node Architecture





Prototype



2nd Generation

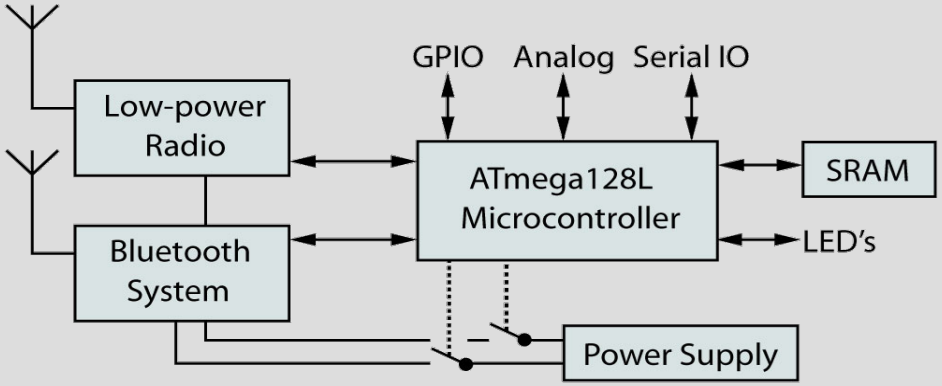
3rd Generation

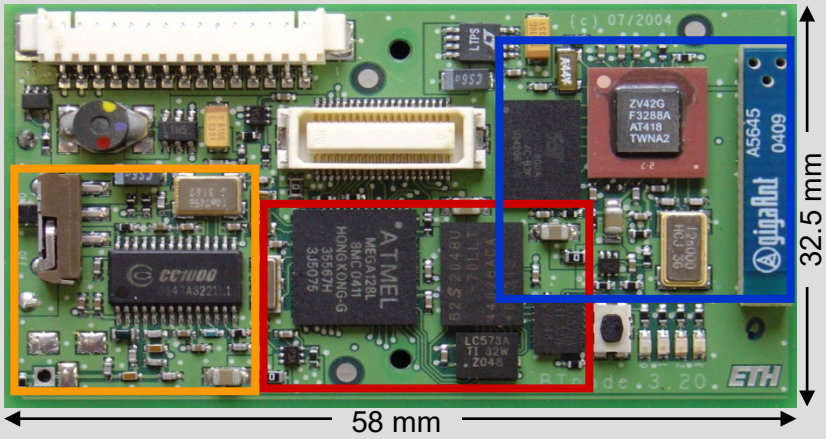
BTnode rev3 Architecture Details

- **System core**
  - Atmel ATmega128
  - 256 kB SRAM
  - Generic IO/Peripherals
  - Switchable power supplies

- Dual radio system

- **Bluetooth radio**
  - 2.4 GHz Zeevo ZV4002
- **Low-power radio**
  - 433-915 MHz ISM Chipcon CC1000





Basic Concepts of WSN Platforms

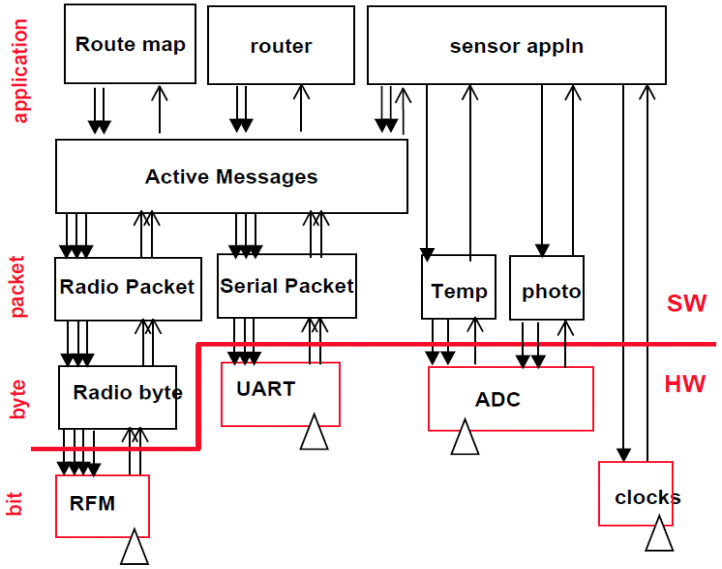
- "Mote class" devices
  - Microcontroller + low-power radio
  - Battery powered
  - Many custom applications
  - Large design space, many variants
  - Most prominent examples: Mica2, Mica2Dot, Tmote Sky

- Hardware is packaged with
  - System software and apps
  - Base stations, network access
  - Server-side solutions (backends)
  - Tools (e.g. simulators, virtual machines …)

- First anticipation
  - Small = cheap = low complexity = many is easy

A Popular Software System – TinyOS

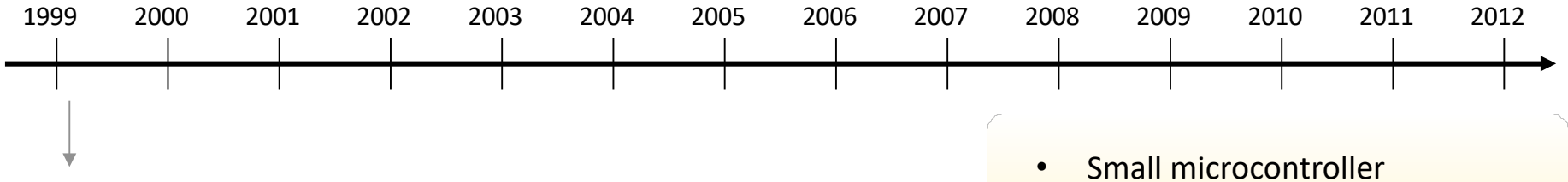
- Event driven “Operating System”
  - Written in nesC, a C dialect
  - Geared towards simple applications (max. 10k RAM, 40 k ROM)
  - Basically just a collection of drivers and an event queuing system
  - Event handlers must not block…
- Compositional nature
  - Hard- and software components
  - Interfaces
  - Modularity
- De-facto standard in WSN applications
  - Popular in academia and industry



- Many (comparable) systems exist: Contiki, SOS, Mantis, BTnut…

WSN Platform Variants

Meet the Family

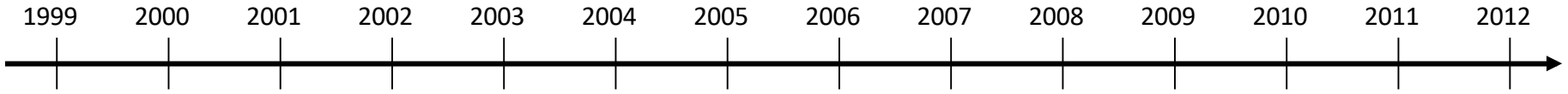


WeC [1999] "Smart Rock"

- Small microcontroller
  - 8 KB Program
  - 512 B Data
- 32 KB EEPROM
- Simple, low-power radio
  - 10 kbps ASK
- Simple sensors
- Active power: 15 mW

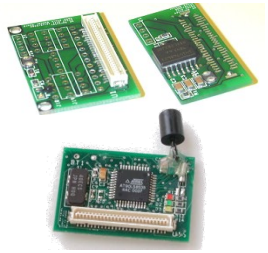
[S. Santini, TU Darmstadt]

Meet the Family



WeC [1999] "Smart Rock"

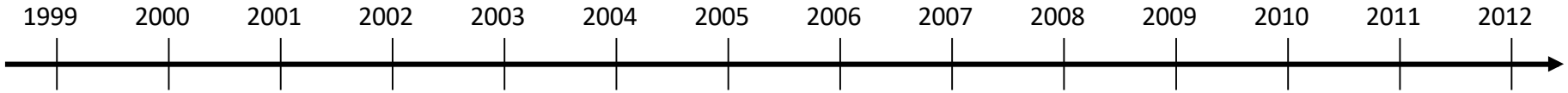
Rene [11/2000]



- Designed for experimentation:
  - Sensor boards
  - Power boards
- Active power: 8 mW

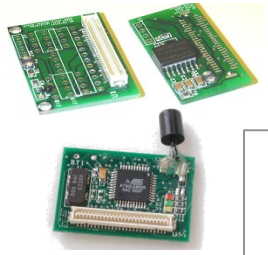
[S. Santini, TU Darmstadt]

Meet the Family



WeC [1999] "Smart Rock"

Rene [11/2000]

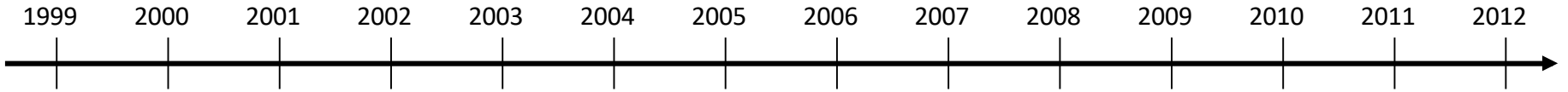


Dot [9/2001]

- Demonstrate scale

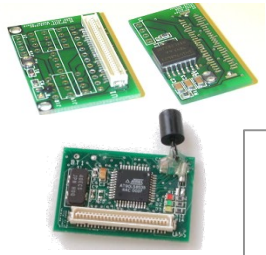
[S. Santini, TU Darmstadt]

Meet the Family

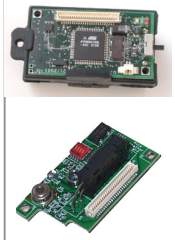


WeC [1999] "Smart Rock"

Rene [11/2000]



Mica [1/2002]

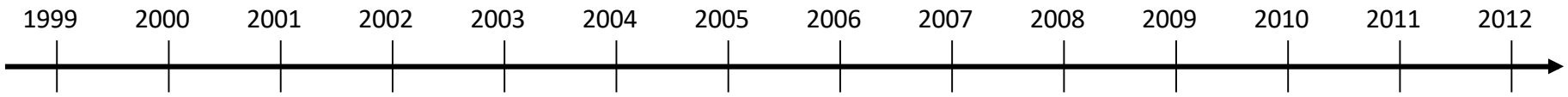


Dot [9/2001]

- NEST program open experimentation platform
  - 128 KB code
  - 4 KB data
- 40 kbps OOK/ASK radio
- 512 KB Flash
- Sensor boards

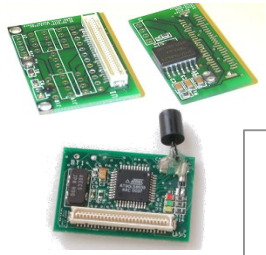
[S. Santini, TU Darmstadt]

Meet the Family



WeC [1999] "Smart Rock"

Rene [11/2000]



Mica [1/2002]

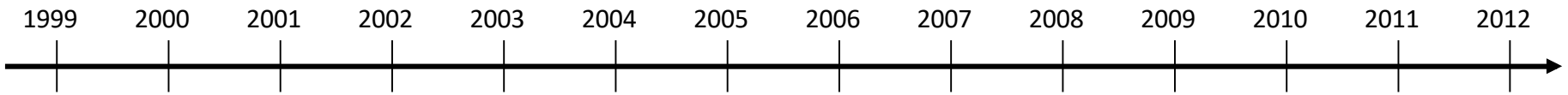
Mica2 [12/2002]

Dot [9/2001]

- Commercial platform
  - 128 KB code
  - 4 KB data
- 38.4 kbps FSK radio
- 512 KB Flash
- Active power: 33 mW

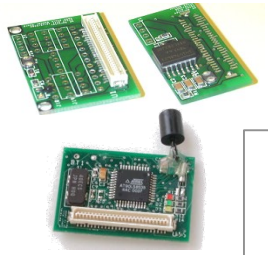
[S. Santini, TU Darmstadt]

Meet the Family



WeC [1999] "Smart Rock"

Rene [11/2000]

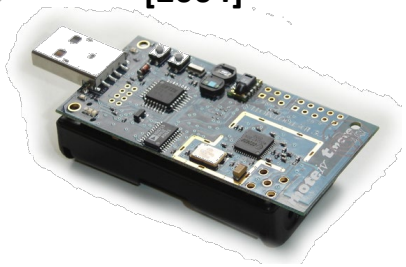


Mica [1/2002]

Mica2 [12/2002]

Dot [9/2001]

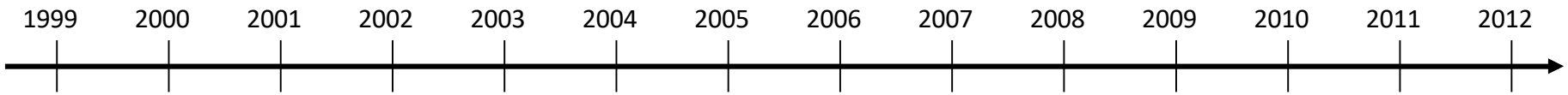
Telos [2004]



- Robust low power operation
- 8 MHz TI MSP430
  - 48 KB code
  - 10 KB RAM
- 1 MB External Flash
- Chipcon 802.15.4 radio
- CPU active power: 3 mW
- Peak current draw, radio active: 21.8mA or ~50-60mW

[S. Santini, TU Darmstadt]

Meet the Family



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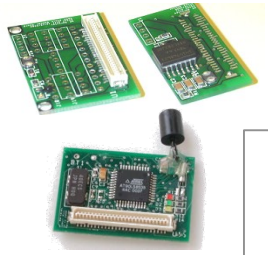

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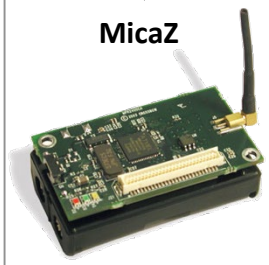
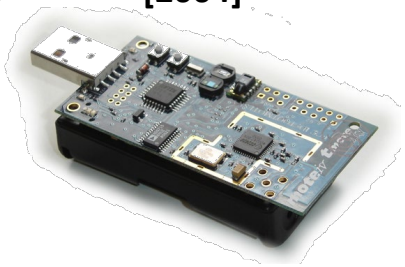
Mica2 [12/2002]

Dot [9/2001]

MicaZ



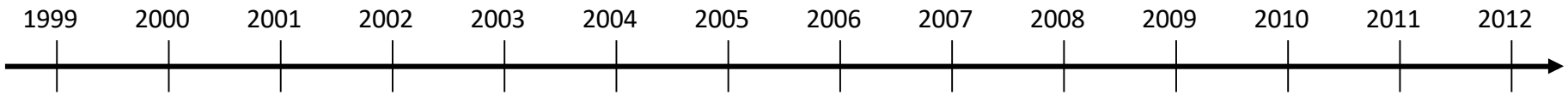
Telos [2004]



- Extension of first commercial product
  - 128 KB code
  - 4 KB data
- 512 KB Flash
- 250 kbps 802.15.4 compliant radio

[S. Santini, TU Darmstadt]

Meet the Family



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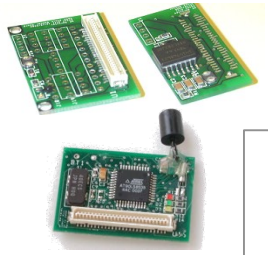

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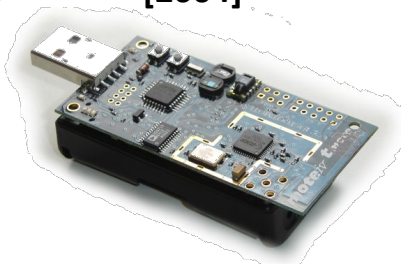

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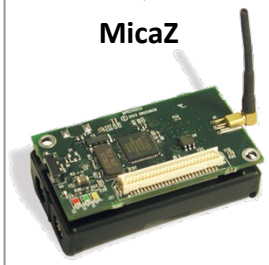
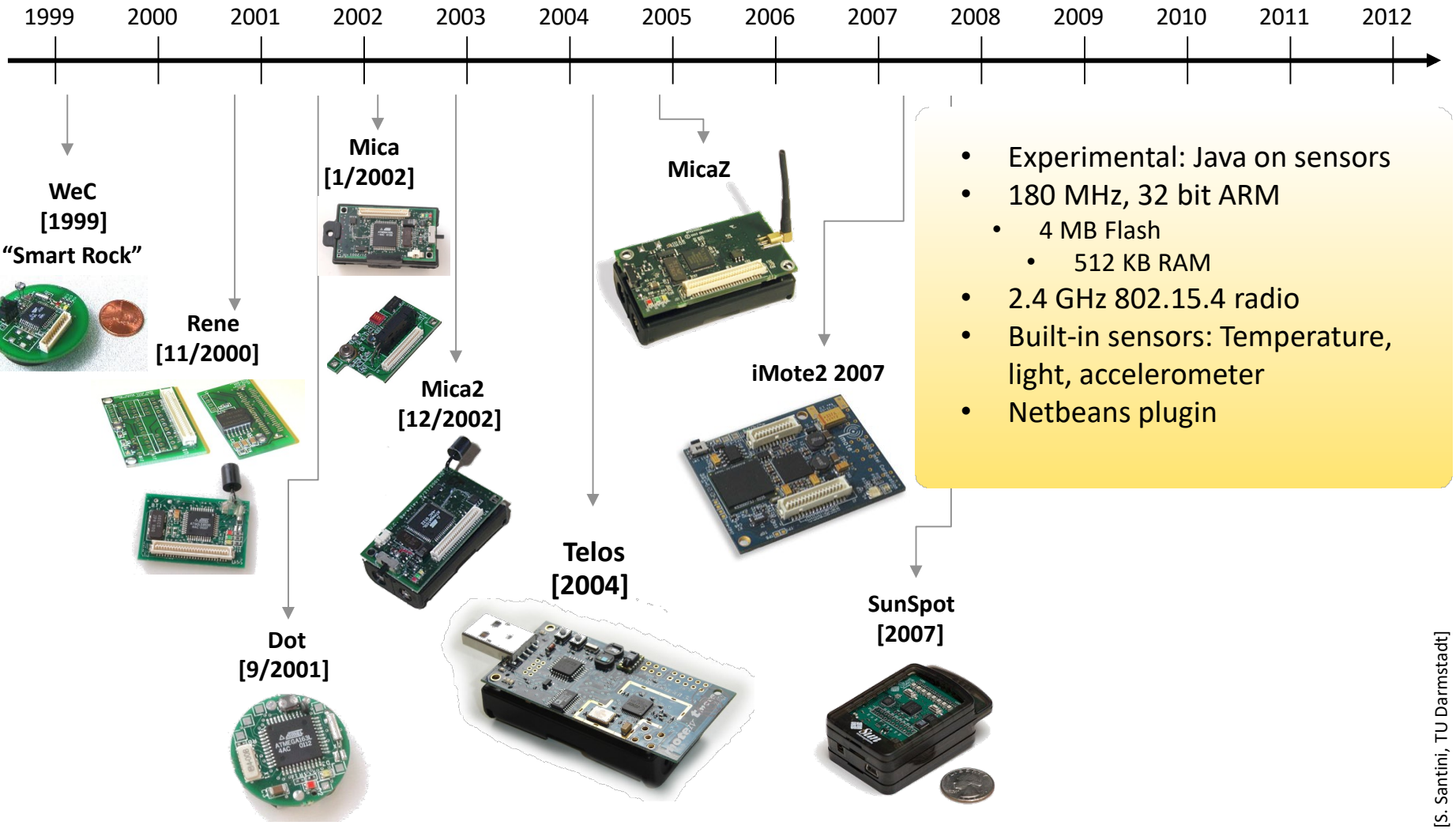


iMote2 2007

- Processor-intensive apps
- Intel XScale CPU, 13~416MHz
  - 32 MB SDRAM
  - 256 KB RAM
- 32 MB Flash
- Wireless MMX DSP co-proc
- 2.4 GHz 802.15.4 Radio
- Camera interface

[S. Santini, TU Darmstadt]

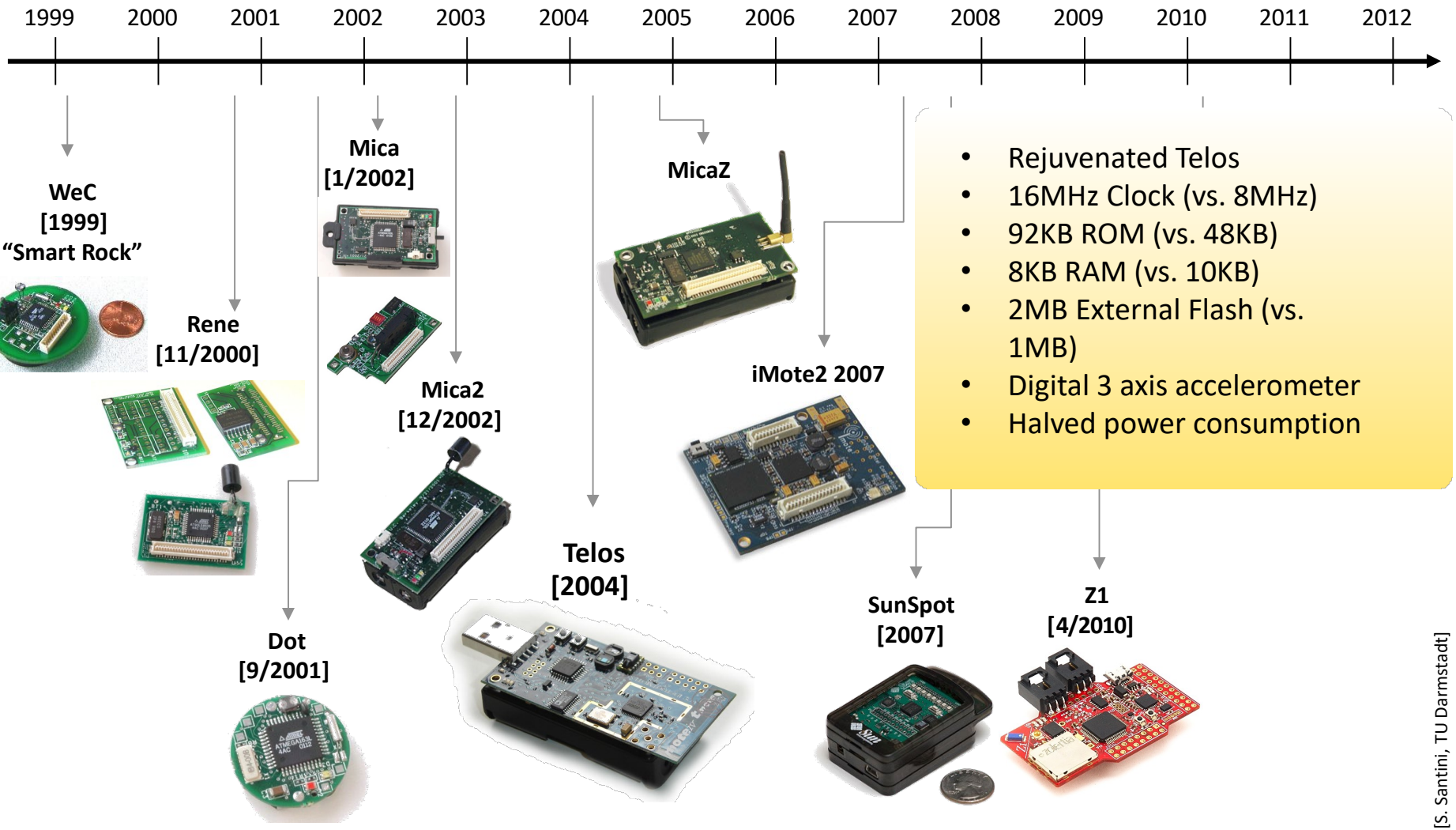
Meet the Family



- Experimental: Java on sensors
- 180 MHz, 32 bit ARM
  - 4 MB Flash
    - 512 KB RAM
- 2.4 GHz 802.15.4 radio
- Built-in sensors: Temperature, light, accelerometer
- Netbeans plugin

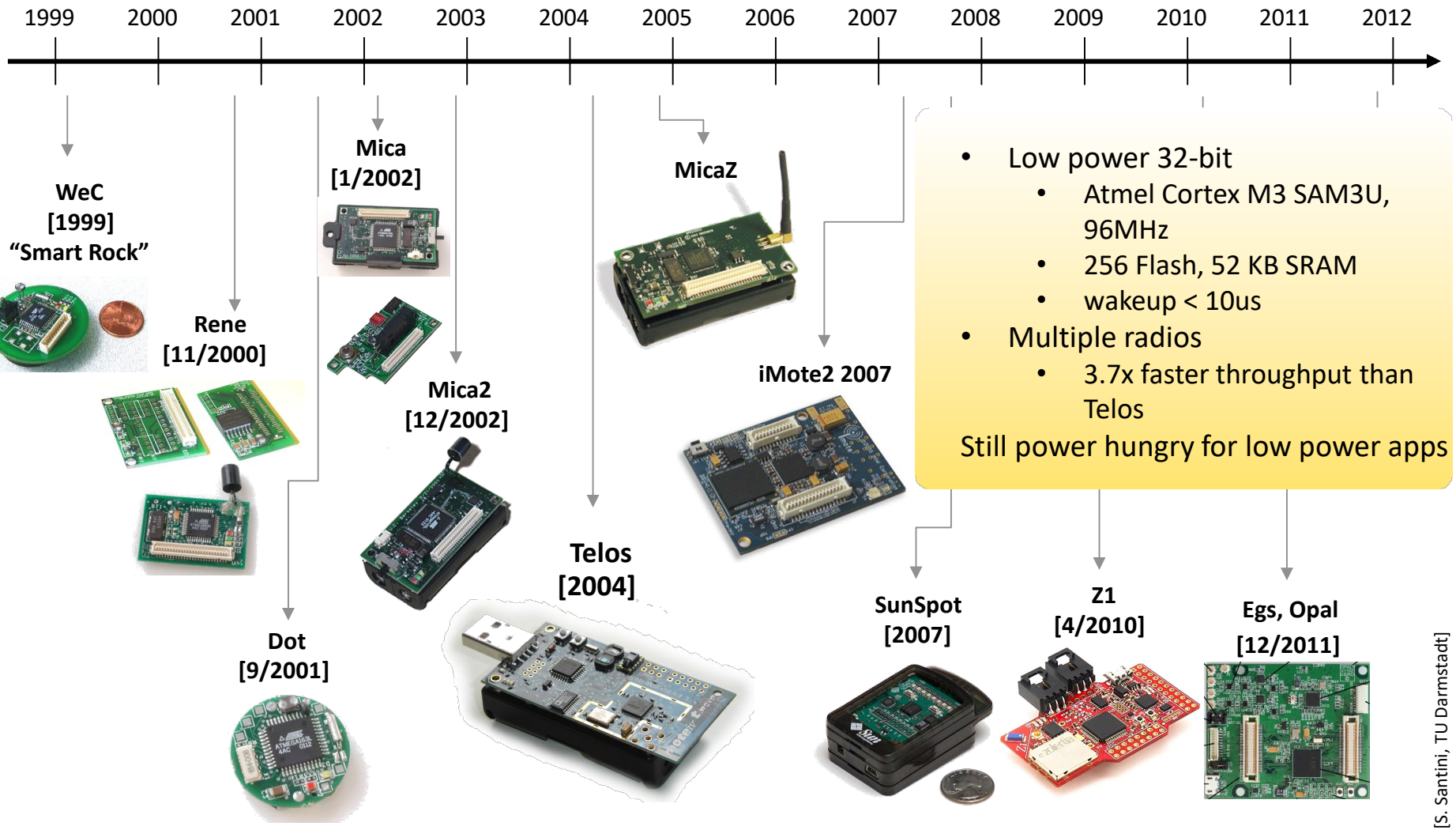
[S. Santini, TU Darmstadt]

Meet the Family



[S. Santini, TU Darmstadt]

Meet the Family

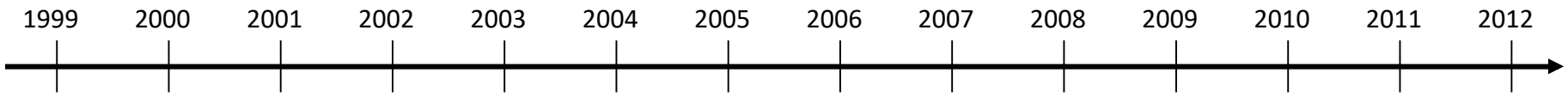


- Low power 32-bit
  - Atmel Cortex M3 SAM3U, 96MHz
  - 256 Flash, 52 KB SRAM
  - wakeup < 10us
- Multiple radios
  - 3.7x faster throughput than Telos

Still power hungry for low power apps

[S. Santini, TU Darmstadt]

Meet the Family



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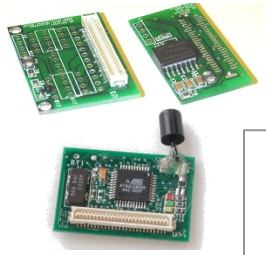

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Mica2 [12/2002]

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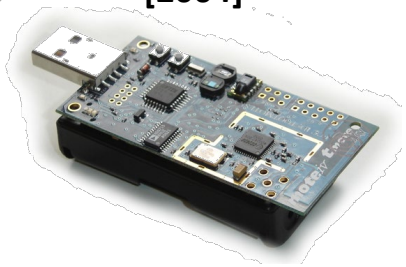
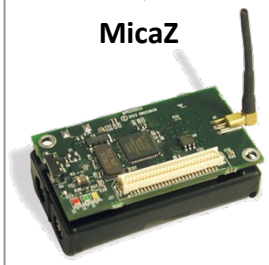


MicaZ

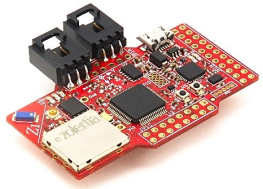


iMote2 2007

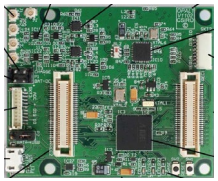
- Two 32-bit microcontrollers
  - Jennic JN5148 SoC
  - 16MHz, 128KB RAM, 128KB ROM
  - ATmega 324
- 36mA in active mode
- SD-card slot
- USB-capabilities
- Wireless inertial motion tracking

SunSpot [2007]

Z1 [4/2010]



Egs, Opal [12/2011]



jNode [2012]

Low-Power System Design

LOW-POWER SYSTEM ARCHITECTURES

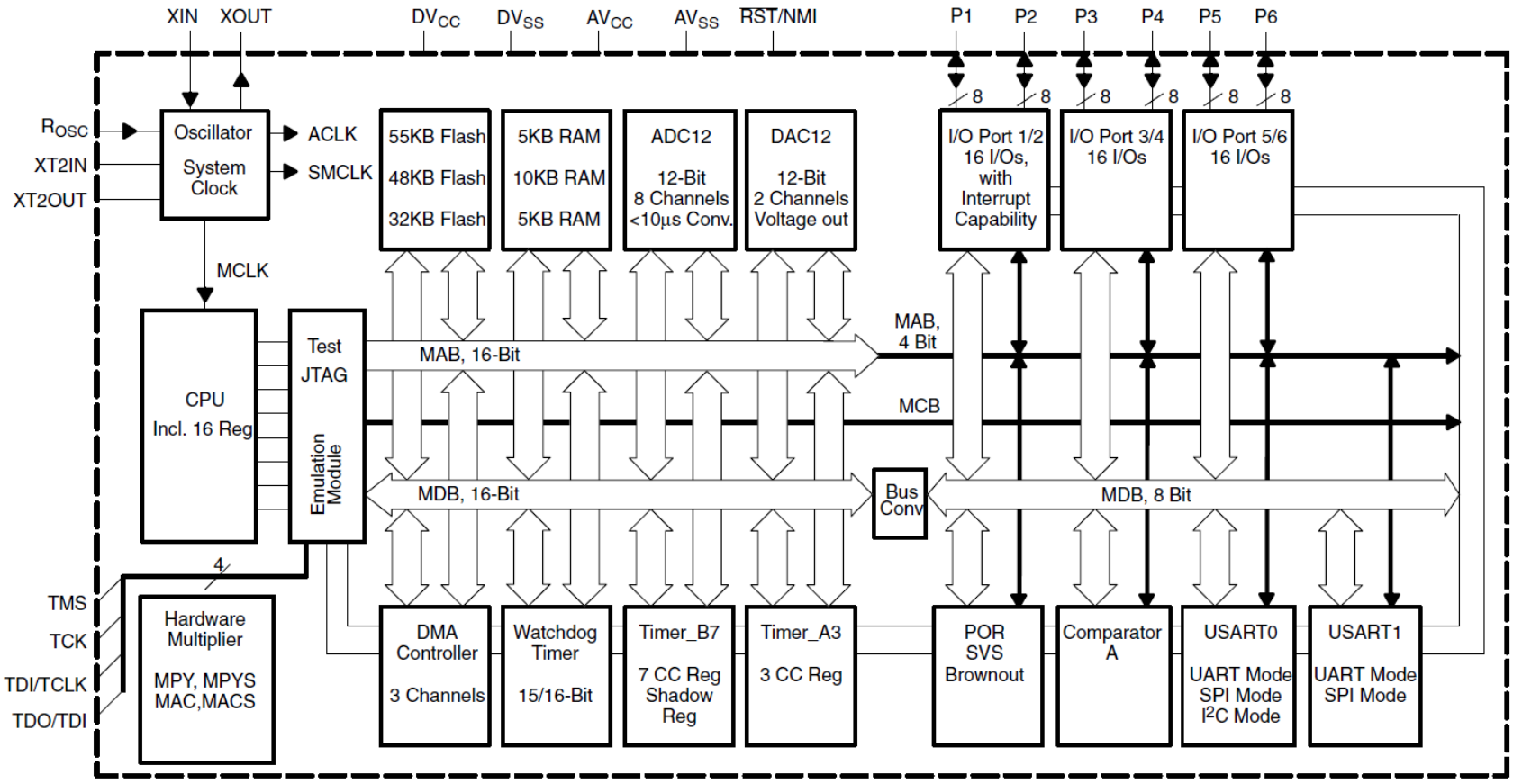
MSP430x161x Specs

- Low Supply-Voltage Range, 1.8 V . . . 3.6 V
- Ultralow-Power Consumption:
  - Active Mode: 330 μA at 1 MHz, 2.2 V
  - Standby Mode: 1.1 μA
  - Off Mode (RAM Retention): 0.2 μA
- Five Power-Saving Modes
- Wake-Up From Standby Mode in less than 6 μs
- 16-Bit RISC Architecture, 125-ns Instruction Cycle Time
- Three-Channel Internal DMA
- 12-Bit A/D Converter With Internal Reference, Sample-and-Hold and Autoscan Feature
- Dual 12-Bit D/A Converters With Synchronization
- 16-Bit Timer_A With Three Capture/Compare Registers
- 16-Bit Timer_B With Three or Seven Capture/Compare-With-Shadow Registers
- On-Chip Comparator
- Serial Communication Interface (USART0), Functions as Asynchronous UART or Synchronous SPI or I^2C^{TM} Interface
- Serial Communication Interface (USART1), Functions as Asynchronous UART or Synchronous SPI Interface
- Supply Voltage Supervisor/Monitor With Programmable Level Detection
- Serial Onboard Programming, No External Programming Voltage Needed Programmable Code Protection by Security Fuse
- Family Members Include:
  - MSP430F155:
    16KB+256B Flash Memory
    512B RAM
  - MSP430F156:
    24KB+256B Flash Memory
    1KB RAM
  - MSP430F157:
    32KB+256B Flash Memory,
    1KB RAM
  - MSP430F167:
    32KB+256B Flash Memory,
    1KB RAM
  - MSP430F168:
    48KB+256B Flash Memory,
    2KB RAM

Tmote Sky [Polastre etal.]

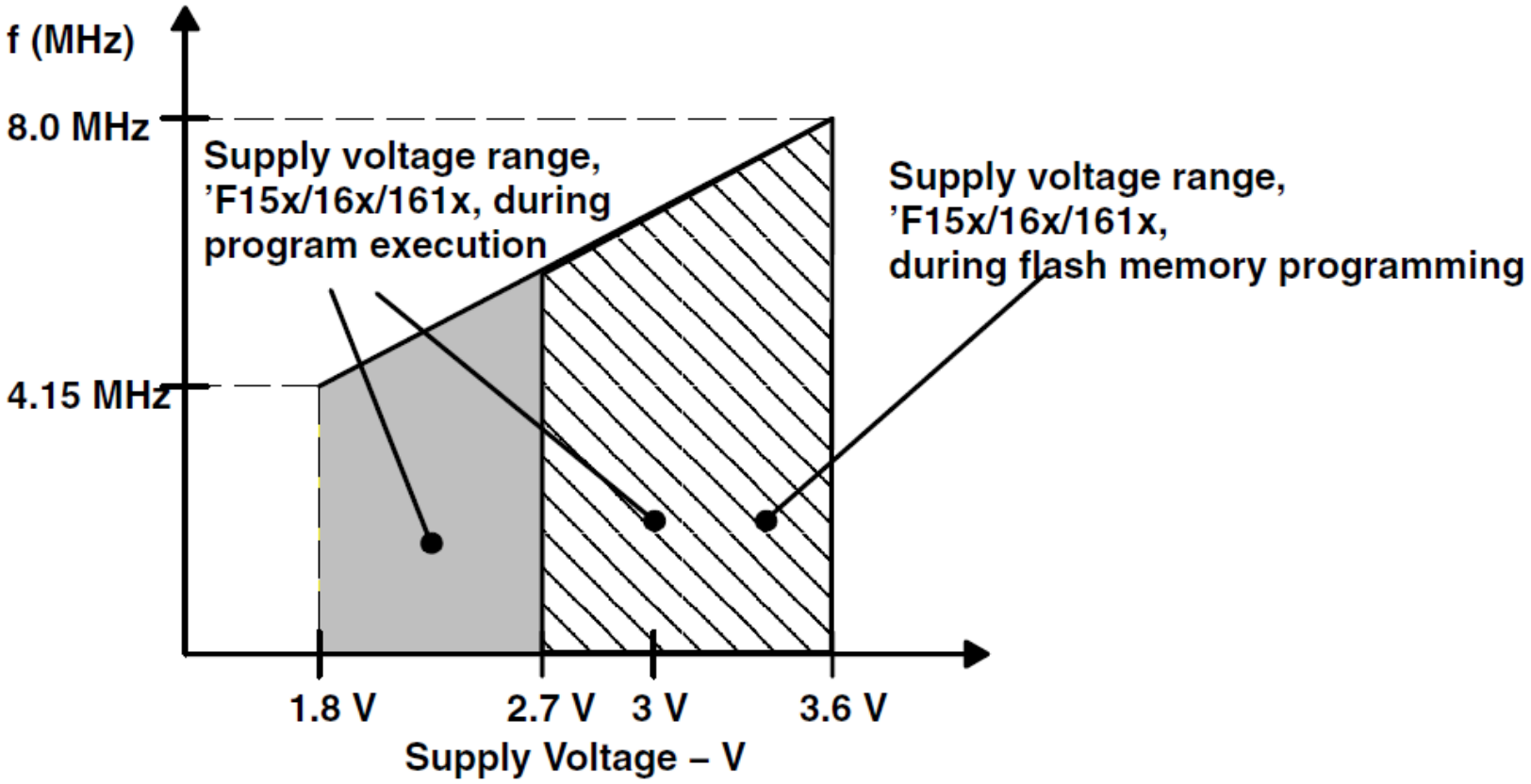
[Texas Instruments]

MSP430x161x Internals



[Texas Instruments]

Frequency vs. Supply Voltage Max Range



[Texas Instruments]

Estimating Frequency and Voltage Effects

- Dynamic power (switching power) dissipated per unit of time

$$P = C \cdot V^2 \cdot A \cdot f$$

- Current consumption of active mode versus system frequency

$$I_{(AM)} = I_{(AM)}\ [1\ \text{MHz}] \times f(\text{System})\ [\text{MHz}]$$

- Current consumption of active mode versus supply voltage

$$I_{(AM)} = I_{(AM)}\ [3\ \text{V}] + 210\ \mu\text{A/V} \times (\text{VCC} - 3\ \text{V})$$

- Example:
  - $f_{(SMCLK)} = 1\ \text{MHz}$; Vcc = 2.2V => Nominal $I_{(AM)} = 330\ \text{uA}$

[Texas Instruments]

LP Mode Standard Operating Conditions

MSP430F161x supply current into AV_{CC} + DV_{CC} excluding external current (AV_{CC} = DV_{CC} = V_{CC})

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
$I_{(AM)}$	Active mode, (see Note 1) $f_{(MCLK)}$ = $f_{(SMCLK)}$ = 1 MHz, $f_{(ACLK)}$ = 32,768 Hz XTS=0, SELM=(0,1)	T_A = –40°C to 85°C	V_{CC} = 2.2 V		330	400	µA
			V_{CC} = 3 V		500	600	
	Active mode, (see Note 1) $f_{(MCLK)}$ = $f_{(SMCLK)}$ = 4,096 Hz, $f_{(ACLK)}$ = 4,096 Hz XTS=0, SELM=3	T_A = –40°C to 85°C	V_{CC} = 2.2 V		2.5	7	µA
			V_{CC} = 3 V		9	20	
$I_{(LPM0)}$	Low-power mode, (LPM0) $f_{(MCLK)}$ = 0 MHz, $f_{(SMCLK)}$ = 1 MHz, $f_{(ACLK)}$ = 32,768 Hz XTS=0, SELM=(0,1) (see Note 1)	T_A = –40°C to 85°C	V_{CC} = 2.2 V		50	60	µA
			V_{CC} = 3 V		75	95	
$I_{(LPM2)}$	Low-power mode, (LPM2), $f_{(MCLK)}$ = $f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 32.768 Hz, SCG0 = 0	T_A = –40°C to 85°C	V_{CC} = 2.2 V		11	14	µA
			V_{CC} = 3 V		17	22	
$I_{(LPM3)}$	Low-power mode, (LPM3) $f_{(MCLK)}$ = $f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 32,768 Hz, SCG0 = 1 (see Note 2)	T_A = –40°C	V_{CC} = 2.2 V		1.3	1.6	µA
		T_A = 25°C			1.3	1.6	
		T_A = 85°C			3.0	6.0	
		T_A = –40°C	V_{CC} = 3 V		2.6	3.0	
		T_A = 25°C			2.6	3.0	
		T_A = 85°C			4.4	8.0	
$I_{(LPM4)}$	Low-power mode, (LPM4) $f_{(MCLK)}$ = 0 MHz, $f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 0 Hz, SCG0 = 1	T_A = –40°C	V_{CC} = 2.2V / 3 V		0.2	0.5	µA
		T_A = 25°C			0.2	0.5	
		T_A = 85°C			2.0	5.0	

NOTES: 1. Timer_B is clocked by $f_{(DCOCLK)}$ = 1 MHz. All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
2. WDT is clocked by $f_{(ACLK)}$ = 32,768 Hz. All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current. The current consumption in LPM2 and LPM3 are measured with ACLK selected.

[Texas Instruments]

MSP430x161x Low Power Modes

- Active mode AM
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
  - ACLK and SMCLK remain active. MCLK is disabled
- Low-power mode 1 (LPM1)
  - CPU is disabled
  - ACLK and SMCLK remain active. MCLK is disabled
  - DCO's dc-generator is disabled if DCO not used in active mode
- Low-power mode 2 (LPM2)
  - CPU is disabled
  - MCLK and SMCLK are disabled
  - DCO's dc-generator remains enabled
  - ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled
  - MCLK and SMCLK are disabled
  - DCO's dc-generator is disabled
  - ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - ACLK is disabled
  - MCLK and SMCLK are disabled
  - DCO's dc-generator is disabled
  - **Crystal oscillator is stopped**

Timer control possible

wake-up LPM3

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(LPM3)}$	Delay time	V_{CC} = 2.2 V/3 V, $f_{DCO} \geq f_{DCO43}$			6	µs

Wakeup only through external IRQ

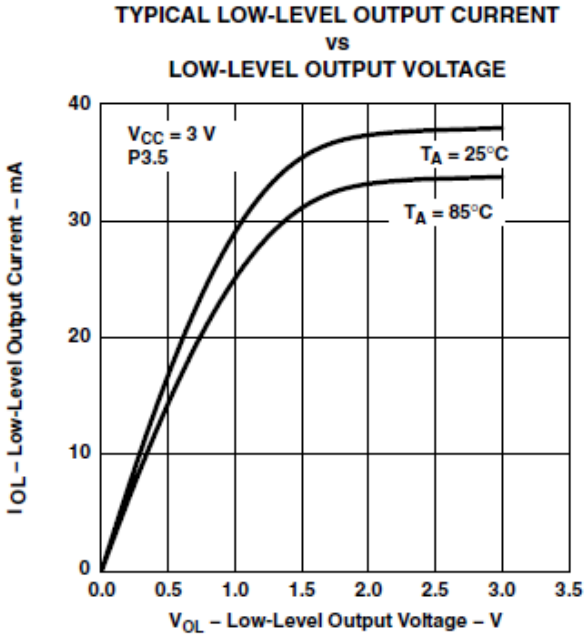
[Texas Instruments]

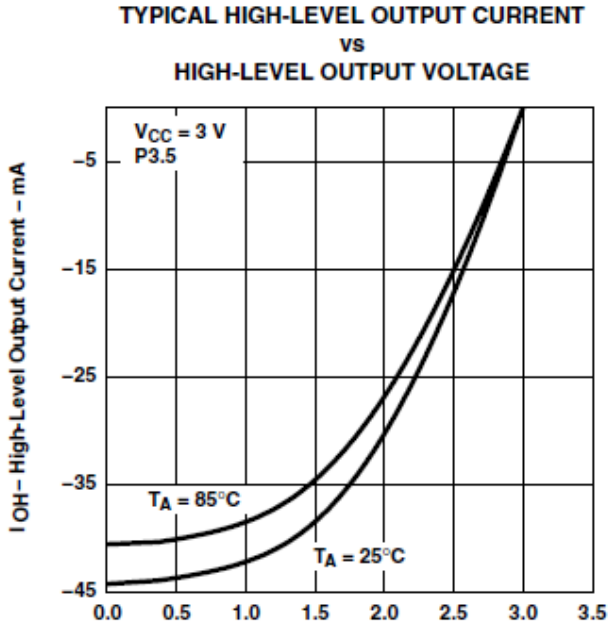
What is External Current?

leakage current – Ports P1, P2, P3, P4, P5 and P6 (see Note 1)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{lkg(Px.y)}$	Leakage current	Port Px	$V_{(Px.y)}$ (see Note 2)	V_{CC} = 2.2 V/3 V			±50	nA

NOTES: 1. The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
2. The port pin must be selected as input.



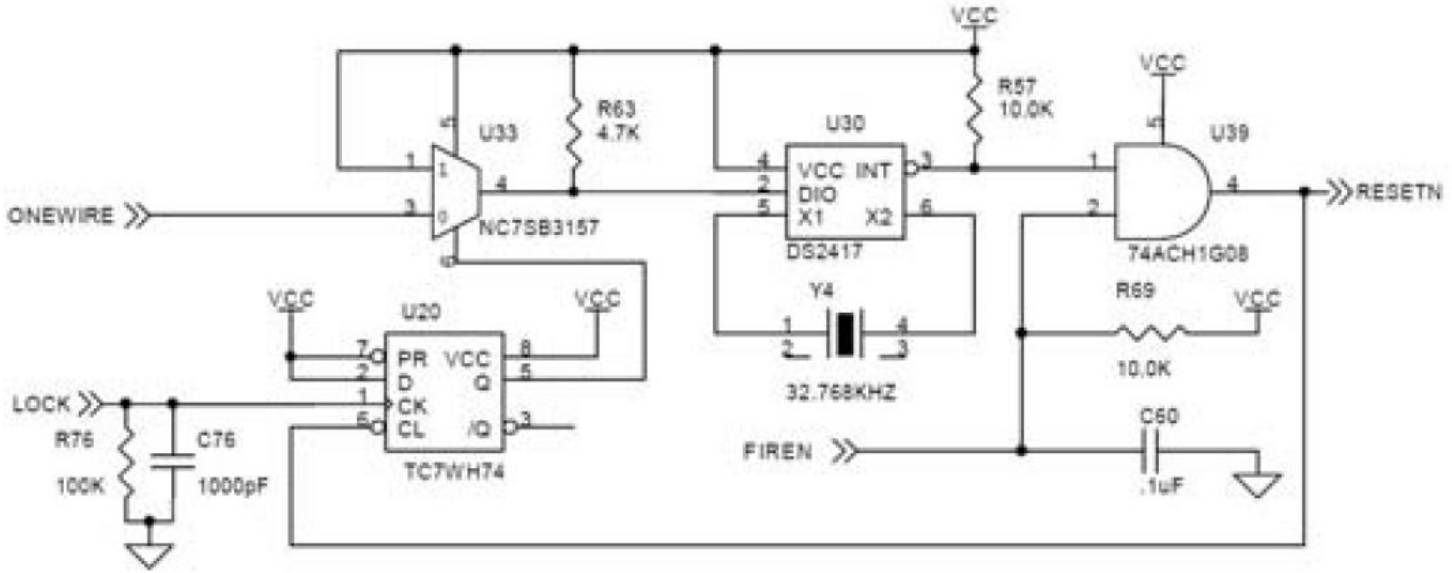


[Texas Instruments]

External Wakeup: XSM Grenade Timer

- External clock circuit triggering IRQ-based wakeup
  - DS2417 I_{cc}=2 uA
  - D-FlipFlop I_{cc}=2.0 uA @ 25°C, max. 20uA @ -40-85°C
  - Other logic…
  - Today this is integrated in modern SOCs

Dutta, P., Grimmer, M., Arora, A., Bibykt, S., & Culler, D. (2005). Design of a wireless sensor network platform for detecting rare, random, and ephemeral events. IPSN 2005 (Vol. 2005, pp. 497–502).



[image P. Dutta, U Michigan]

MSP Family Variant: MSP430x241x

- Low Supply-Voltage Range, 1.8 V to 3.6 V
- Ultralow-Power Consumption:
  - Active Mode: 365 μA at 1 MHz, 2.2 V
  - Standby Mode (VLO): 0.5 μA
  - Off Mode (RAM Retention): 0.1 μA
- Wake-Up From Standby Mode in Less Than 1 μs
- 16-Bit RISC Architecture, 62.5-nsInstruction Cycle Time
- Three-Channel Internal DMA
- 12-Bit Analog-to-Digital (A/D) Converter With Internal Reference, Sample-and-Hold, and Autoscan Feature
- Dual 12-Bit Digital-to-Analog (D/A) Converters With Synchronization
- 16-Bit Timer_A With Three Capture/Compare Registers
- 16-Bit Timer_B With Seven Capture/Compare-With-Shadow Registers
- On-Chip Comparator
- Four Universal Serial Communication Interfaces (USCIs)
  - USCI_A0 and USCI_A1
    - Enhanced UART Supporting Auto-Baudrate Detection
    - IrDA Encoder and Decoder
    - Synchronous SPI
  - USCI_B0 and USCI_B1
    - I^2C™
    - Synchronous SPI
- Supply Voltage Supervisor/Monitor With Programmable Level Detection
- Brownout Detector
- Bootstrap Loader
- Serial Onboard Programming, No External Programming Voltage Needed Programmable Code Protection by Security Fuse
- Family Members Include:
  - MSP430F2416: 92KB+256B Flash Memory, 4KB RAM
  - MSP430F2417: 92KB+256B Flash Memory, 8KB RAM
  - MSP430F2418: 116KB+256B Flash Memory, 8KB RAM
  - MSP430F2419: 120KB+256B Flash Memory, 4KB RAM
  - MSP430F2616: 92KB+256B Flash Memory, 4KB RAM
  - MSP430F2617: 92KB+256B Flash Memory, 8KB RAM
  - MSP430F2618: 116KB+256B Flash Memory, 8KB RAM
  - MSP430F2619: 120KB+256B Flash Memory, 4KB RAM
- Available in 80-Pin Quad Flat Pack (QFP) and 64-Pin QFP (See Available Options)
- For Complete Module Descriptions, See the *MSP430x2xx Family User's Guide*, Literature Number SLAU144

† The MSP430F241x devices are identical to the MSP430F261x devices, with the exception that the DAC12 modules and the DMA controller are not implemented.

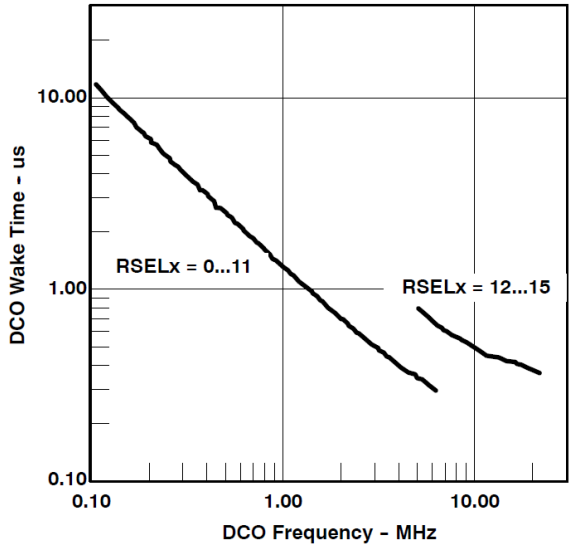
[Texas Instruments]

What Really Changed?

wake-up from low-power modes (LPM3/LPM4)

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
$t_{DCO,LPM3/4}$	DCO clock wake-up time from LPM3/4 (see Note 1)	BCSCTL1= CALBC1_1MHz, DCOCTL = CALDCO_1MHz	2.2 V/3 V			2	µs
		BCSCTL1= CALBC1_8MHz, DCOCTL = CALDCO_8MHz	2.2 V/3 V			1.5	
		BCSCTL1= CALBC1_12MHz, DCOCTL = CALDCO_12MHz	2.2 V/3 V			1	
		BCSCTL1= CALBC1_16MHz, DCOCTL = CALDCO_16MHz	3 V			1	
$t_{CPU,LPM3/4}$	CPU wake-up time from LPM3/4 (see Note 2)				$1/f_{MCLK}$ + $t_{Clock,LPM3/4}$		

NOTES: 1. The DCO clock wake-up time is measured from the edge of an external wake-up signal (e.g., port interrupt) to the first clock edge observable externally on a clock pin (MCLK or SMCLK).
2. Parameter applicable only if DCOCLK is used for MCLK.



[Texas Instruments]

MSP430x161x Memory Subsystem

Flash Memory

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	NOM	MAX	UNIT
$V_{CC(PGM/ERASE)}$	Program and Erase supply voltage			2.7		3.6	V
f_{FTG}	Flash Timing Generator frequency			257		476	kHz
I_{PGM}	Supply current from DV_{CC} during program		2.7 V/ 3.6 V		3	5	mA
I_{ERASE}	Supply current from DV_{CC} during erase		2.7 V/ 3.6 V		3	7	mA
t_{CPT}	Cumulative program time	see Note 1	2.7 V/ 3.6 V			4	ms
$t_{CMErase}$	Cumulative mass erase time	see Note 2	2.7 V/ 3.6 V	200			ms
	Program/Erase endurance			10^4	10^5		cycles
$t_{Retention}$	Data retention duration	T_J = 25°C		100			years
t_{Word}	Word or byte program time	see Note 3			35		t_{FTG}
$t_{Block, 0}$	Block program time for 1st byte or word				30		
$t_{Block, 1-63}$	Block program time for each additional byte or word				21		
$t_{Block, End}$	Block program end-sequence wait time				6		
$t_{Mass Erase}$	Mass erase time				5297		
$t_{Seg Erase}$	Segment erase time				4819		

NOTES:
1. The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
2. The mass erase duration generated by the flash timing generator is at least 11.1ms (= 5297x1/f_{FTG},max = 5297x1/476kHz). To achieve the required cumulative mass erase time the Flash Controller's mass erase operation can be repeated until this time is met. (A worst case minimum of 19 cycles are required).
3. These values are hardwired into the Flash Controller's state machine (t_{FTG} = 1/f_{FTG}).

[Texas Instruments]

MSP Family Variant: MSP430FR59xx

- Embedded Microcontroller
  - 16-Bit RISC Architecture up to 16-MHz Clock
  - Wide Supply Voltage Range (1.8 V [1] to 3.6 V)
- Optimized Ultralow-Power Modes

Mode	Consumption (Typical)
Active Mode	103 µA/MHz
Standby (LPM3 With VLO)	0.4 µA
Real-Time Clock (LPM3.5 With Crystal)	0.5 µA
Shutdown (LPM4.5)	0.02 µA

- Ultralow-Power Ferroelectric RAM (FRAM)
  - Up to 64KB Nonvolatile Memory
  - Ultralow-Power Writes
  - Fast Write at 125 ns Per Word (64KB in 4 ms)
  - Unified Memory = Program + Data + Storage in One Single Space
  - 10^{15} Write Cycle Endurance
  - Radiation Resistant and Nonmagnetic
- Intelligent Digital Peripherals
  - 32-Bit Hardware Multiplier (MPY)
  - Three-Channel Internal DMA
  - Real-Time Clock (RTC) With Calendar and Alarm Functions
  - Five 16-Bit Timers With up to Seven Capture/Compare Registers Each
  - 16-Bit Cyclic Redundancy Checker (CRC)
- High-Performance Analog
  - 16-Channel Analog Comparator
  - 14-Channel 12-Bit Analog-to-Digital Converter (ADC) With Internal Reference and Sample-and-Hold
    - 200 ksps at 75-µA Consumption
- Multifunction Input/Output Ports
  - All Pins Support Capacitive Touch Capability With No Need for External Components
  - Accessible Bit-, Byte-, and Word-Wise (in Pairs)
  - Edge-Selectable Wake From LPM on All Ports
  - Programmable Pullup and Pulldown on All Ports
- Code Security and Encryption
  - 128-Bit or 256-Bit AES Security Encryption and Decryption Coprocessor (MSP430FR59xx Only)
  - Random Number Seed for Random Number Generation Algorithms
- Enhanced Serial Communication
  - eUSCI_A0 and eUSCI_A1 Support
    - UART With Automatic Baud-Rate Detection
    - IrDA Encode and Decode
    - SPI at Rates up to 10 Mbps
  - eUSCI_B0 Supports
    - I^2C With Multiple Slave Addressing
    - SPI at Rates up to 8 Mbps
  - Hardware UART and I^2C Bootstrap Loader (BSL)
- Flexible Clock System
  - Fixed-Frequency DCO With 10 Selectable Factory-Trimmed Frequencies
  - Low-Power Low-Frequency Internal Clock Source (VLO)
  - 32-kHz Crystals (LFXT)
  - High-Frequency Crystals (HFXT)
- Development Tools and Software
  - Professional Development Environments
  - Development Kit (MSP-TS430RGZ48C)
- Family Members
  - Table 2 Summarizes 18 Variants in 3 Available Package Types
- For Complete Module Descriptions, See the *MSP430FR59xx and MSP430FR58xx Family User's Guide* (SLAU367)

[Texas Instruments]

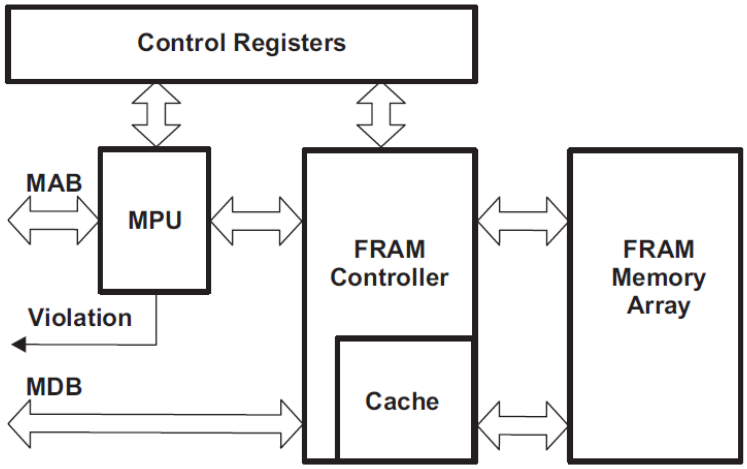
MSP430FRxx Storage Alternative: FRAM

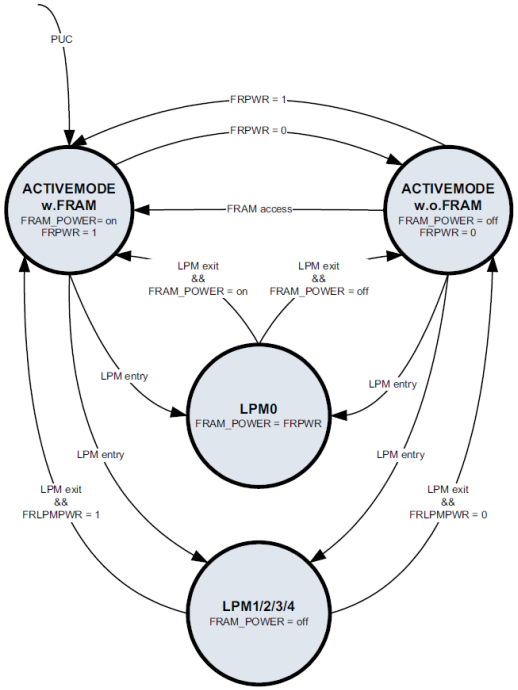
- Ferroelectric RAM (FRAM)
  - Random-access memory similar in construction to DRAM
  - Uses a ferroelectric layer instead of a dielectric layer to achieve non-volatility

- Growing number of alternative non-volatile random-access memory offering the same functionality as flash memory
  - Lower power usage
  - Faster write performance
  - Greater maximum number of write-erase cycles ($>10^{16}$)
  - Lower storage densities
  - Storage capacity limitations
  - Higher cost

FRAM Necessitates a Dedicated Controller

- Byte or word write access
- Automatic and programmable wait state control
- Error correction code (bit errors)
- Cache for fast reads
- Power control when not using FRAM





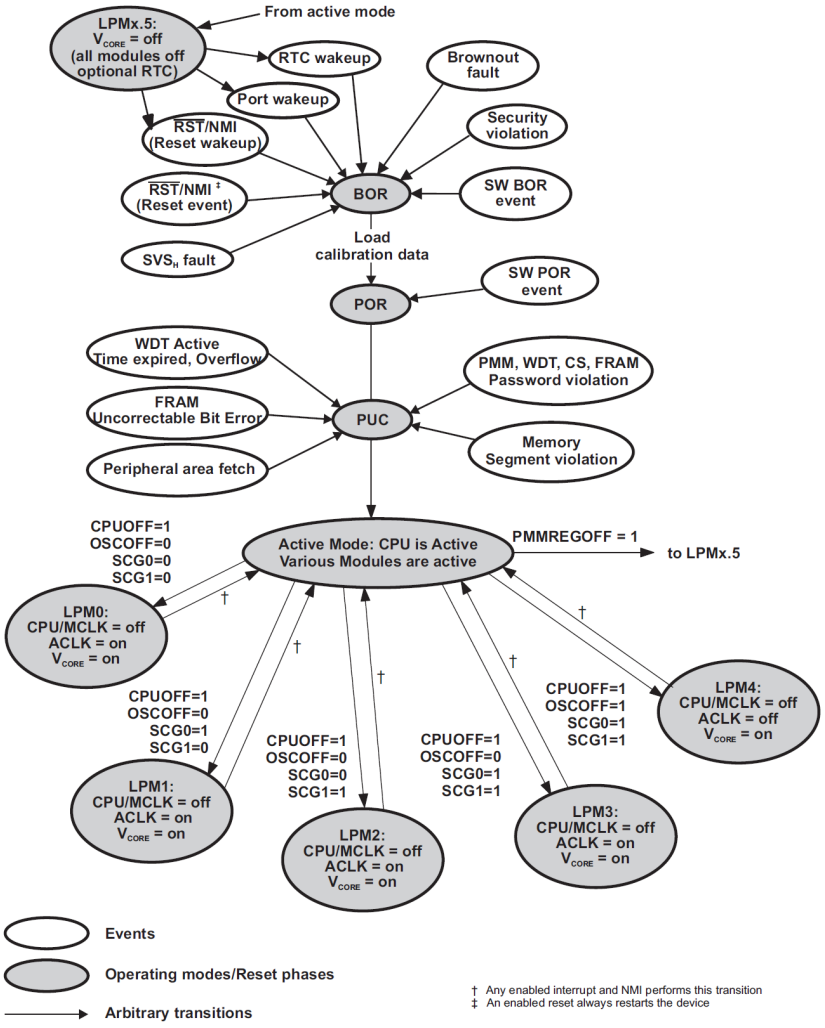
[Texas Instruments]

MSP430FR5969 Low Power Modes

Mode	Active	LPM0	LPM1	LPM2	LPM3	LPM4	LPM4.5
Current @ 1 MHz [µA]	128	86	47	0.81	0.56	0.48	0.04
Current @ 8 MHz [µA]	470	151	112				
Current @ 16 MHz [µA]	855	213	174				
Wake-up delay [µs]	-	0.25	5.75	6	6	6	875 [2]
CPU / FRAM	1	0	0	0	0	0	0
HF / LF / UC Peripherals [1]	1 / 1 / 1	1 / 1 / 1	1 / 1 / 1	0 / 1 / 1	0 / 1 / 1	0 / 0 / 1	0 / 0 / 0
Full retention	1	1	1	1	1	1	0
Wake-up events	-	all	all	I/O comp LF	I/O comp LF	I/O comp	I/O

[1] HF = high frequency (SMCLK), LF = low frequency (ACLK), UC = unclocked (external clock)
[2] not included is the time needed to reinitialize the MCU after the reset

State Transitions: It Looks Straightforward…



[Texas Instruments]

STM32L433xx

[ST Microelectronics]

ETH zürich

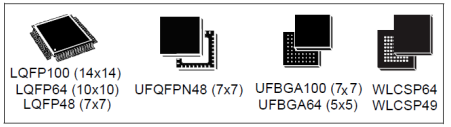
life.augmented

Ultra-low-power Arm® Cortex®-M4 32-bit MCU+FPU, 100DMIPS, up to 256KB Flash, 64KB SRAM, USB FS, LCD, ext. SMPS

Datasheet - production data

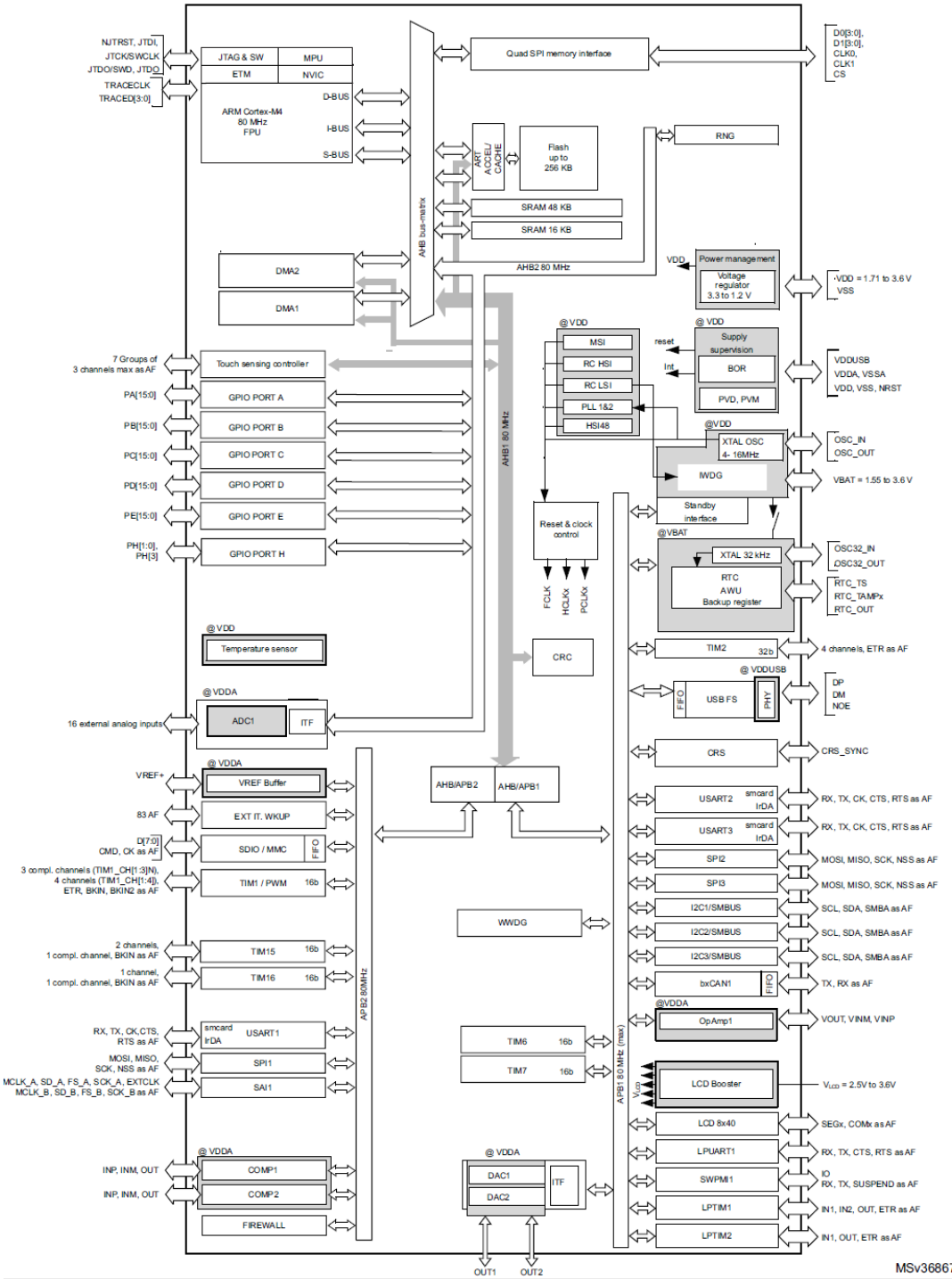
Features

- Ultra-low-power with FlexPowerControl
  - 1.71 V to 3.6 V power supply
  - -40 °C to 85/105/125 °C temperature range
  - 200 nA in V_{BAT} mode: supply for RTC and 32x32-bit backup registers
  - 8 nA Shutdown mode (5 wakeup pins)
  - 28 nA Standby mode (5 wakeup pins)
  - 280 nA Standby mode with RTC
  - 1.0 µA Stop 2 mode, 1.28 µA with RTC
  - 84 µA/MHz run mode (LDO Mode)
  - 36 µA/MHz run mode (@3.3 V SMPS Mode)
  - Batch acquisition mode (BAM)
  - 4 µs wakeup from Stop mode
  - Brown out reset (BOR)
  - Interconnect matrix
- Core: Arm® 32-bit Cortex®-M4 CPU with FPU, Adaptive real-time accelerator (ART Accelerator™) allowing 0-wait-state execution from Flash memory, frequency up to 80 MHz, MPU, 100DMIPS and DSP instructions
- Performance benchmark
  - 1.25 DMIPS/MHz (Drystone 2.1)
  - 273.55 CoreMark® (3.42 CoreMark/MHz @ 80 MHz)
- Energy benchmark
  - 253 ULPBench® score
- Clock Sources
  - 4 to 48 MHz crystal oscillator
  - 32 kHz crystal oscillator for RTC (LSE)
  - Internal 16 MHz factory-trimmed RC (±1%)
  - Internal low-power 32 kHz RC (±5%)
  - Internal multispeed 100 kHz to 48 MHz oscillator, auto-trimmed by LSE (better than ±0.25 % accuracy)
  - Internal 48 MHz with clock recovery
  - 2 PLLs for system clock, USB, audio, ADC



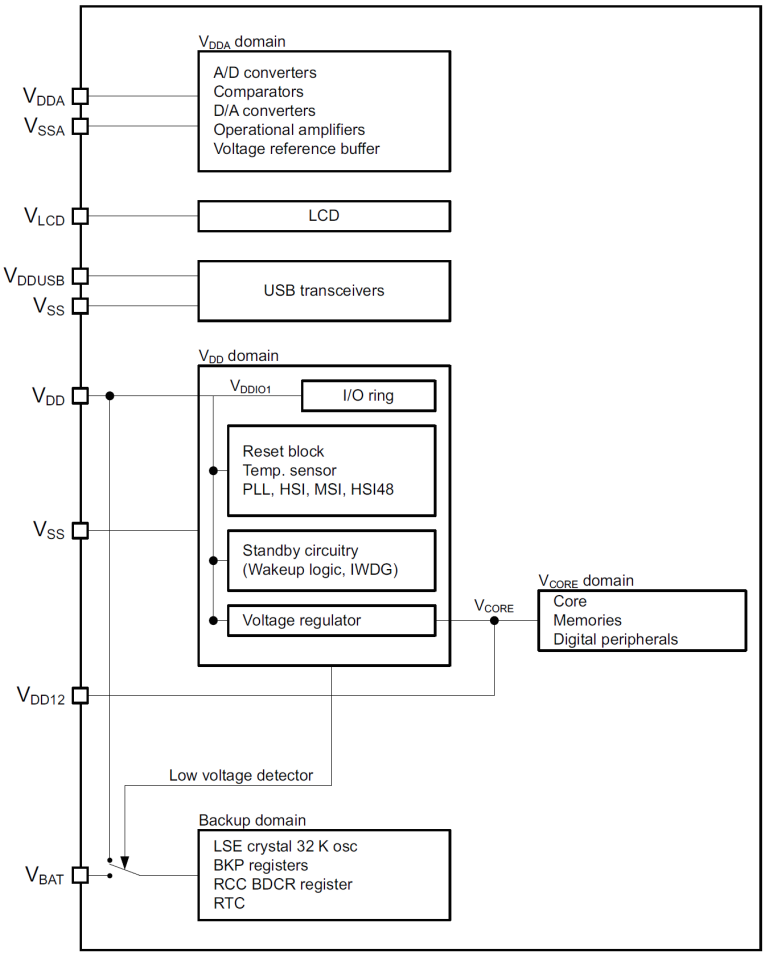
- Up to 83 fast I/Os, most 5 V-tolerant
- RTC with HW calendar, alarms and calibration
- LCD 8× 40 or 4× 44 with step-up converter
- Up to 21 capacitive sensing channels: support touchkey, linear and rotary touch sensors
- 11x timers: 1x 16-bit advanced motor-control, 1x 32-bit and 2x 16-bit general purpose, 2x 16-bit basic, 2x low-power 16-bit timers (available in Stop mode), 2x watchdogs, SysTick timer
- Memories
  - Up to 256 KB single bank Flash, proprietary code readout protection
  - 64 KB of SRAM including 16 KB with hardware parity check
  - Quad SPI memory interface
- Rich analog peripherals (independent supply)
  - 1x 12-bit ADC 5 Msps, up to 16-bit with hardware oversampling, 200 µA/Msps
  - 2x 12-bit DAC output channels, low-power sample and hold
  - 1x operational amplifier with built-in PGA
  - 2x ultra-low-power comparators
- 17x communication interfaces
  - USB 2.0 full-speed crystal less solution with LPM and BCD
  - 1x SAI (serial audio interface)
  - 3x I2C FM+(1 Mbit/s), SMBus/PMBus
  - 4x USARTs (ISO 7816, LIN, IrDA, modem)
  - 1x LPUART (Stop 2 wake-up)
  - 3x SPIs (and 1x Quad SPI)
  - CAN (2.0B Active) and SDMMC interface
  - SWPMI single wire protocol master I/F
  - IRTIM (Infrared interface)

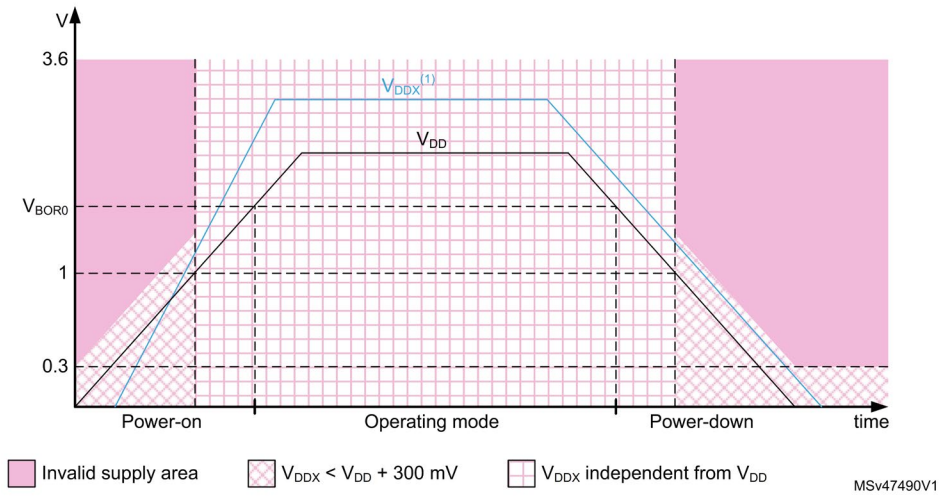
STM32L433xx



[ST Microelectronics]

STM32L433xx





[ST Microelectronics]

Principles for Low-Power Applications

- Reduce power consumption by maximizing time in low-power modes (LPM3 or LPM4)
  - Interrupts to wake the processor and control program flow
  - Peripherals should be switched on only when needed
  - Low-power integrated peripheral modules in place of SW functions
    - Timer_A and Timer_B automatically captures external timing or PWM
    - Direct Memory Access (DMA)
  - Calculated branching and fast table look-ups should be used in place of flag polling and long software calculations
  - Avoid frequent subroutine and function calls due to overhead
  - For longer software routines, single-cycle CPU registers should be used
- For low duty cycles and slow response time events, maximizing time in LPMx.5 can further reduce power

Low-Power System Design

WIRELESS SENSOR NETWORK APPLICATION EXAMPLE

PermaSense

- Interdisciplinary geo-science and engineering collaboration
- Consortium of several projects, start in 2006
- Fundamental as well as applied research
  - Long-term, high-quality sensing in harsh environments
  - Better quality data, obtained online
  - Measurements that have previously been impossible
  - Enabling new science, answering fundamental questions related to decision making, natural hazard early-warning

- More than 35 people, 17 PhD students

FNSNF Fonds national suisse Schweizerischer Nationalfonds Fondo nazionale svizzero Swiss National Science Foundation

nano-tera.ch

NCCR MICS National Competence Center In Research Mobile Information and Communication Systems

Bundesamt für Umwelt BAFU Schweizerische Eidgenossenschaft Confédération suisse Confederazione Svizzera Confederaziun svizra

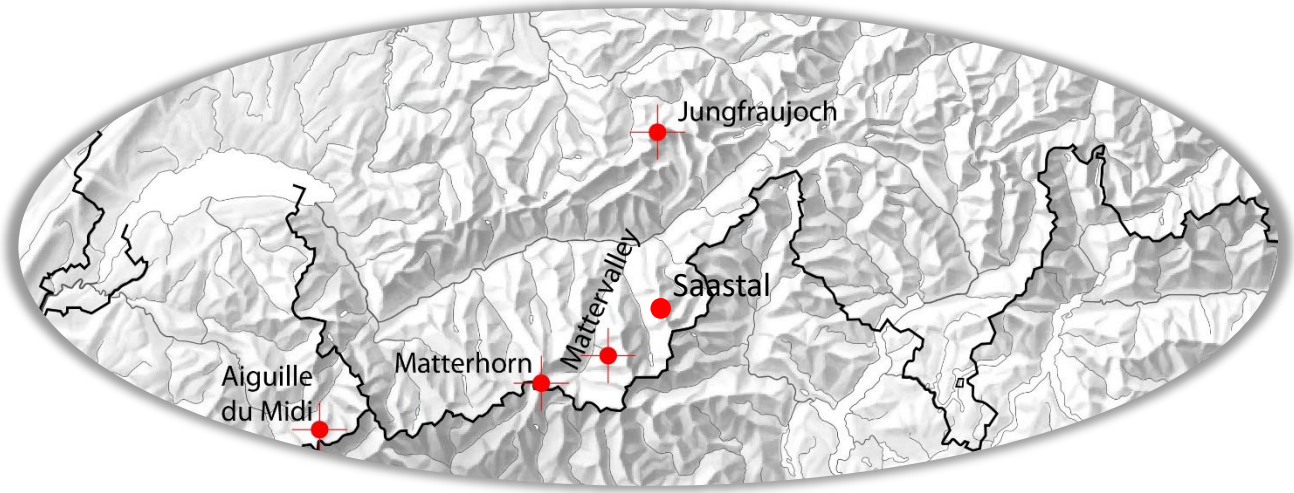
cces

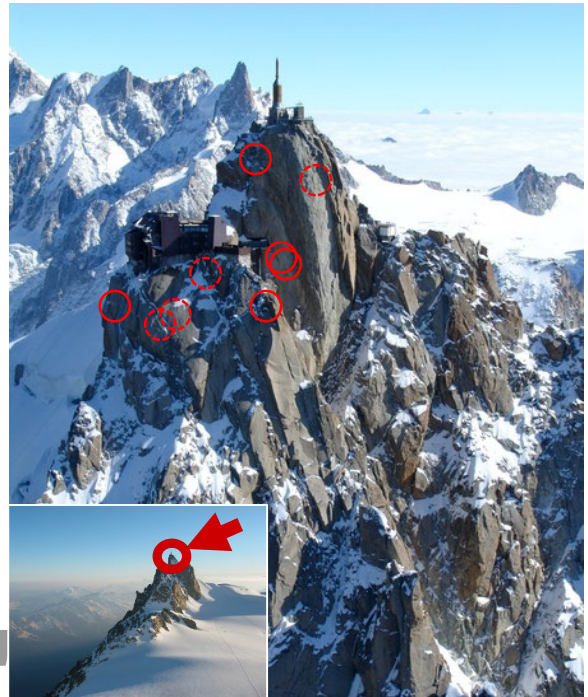
ETH zürich

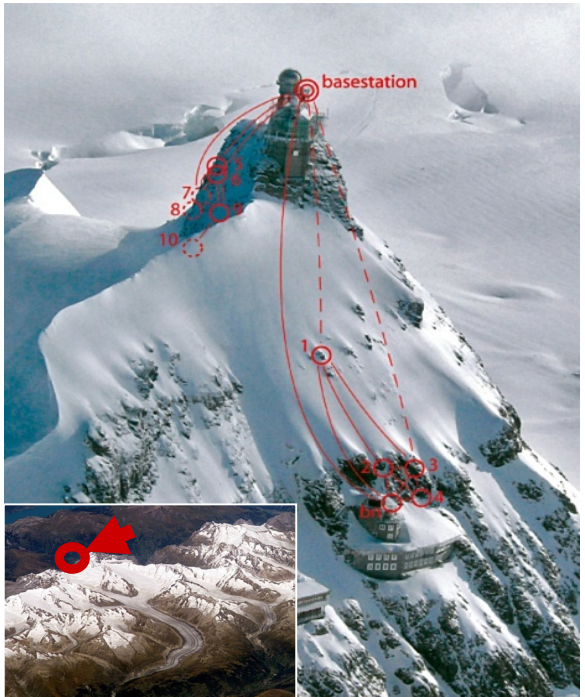

Our patient does not fit into a laboratory


So the laboratory
has to go on the
mountain

Our Field Sites: Precision Scientific Instruments



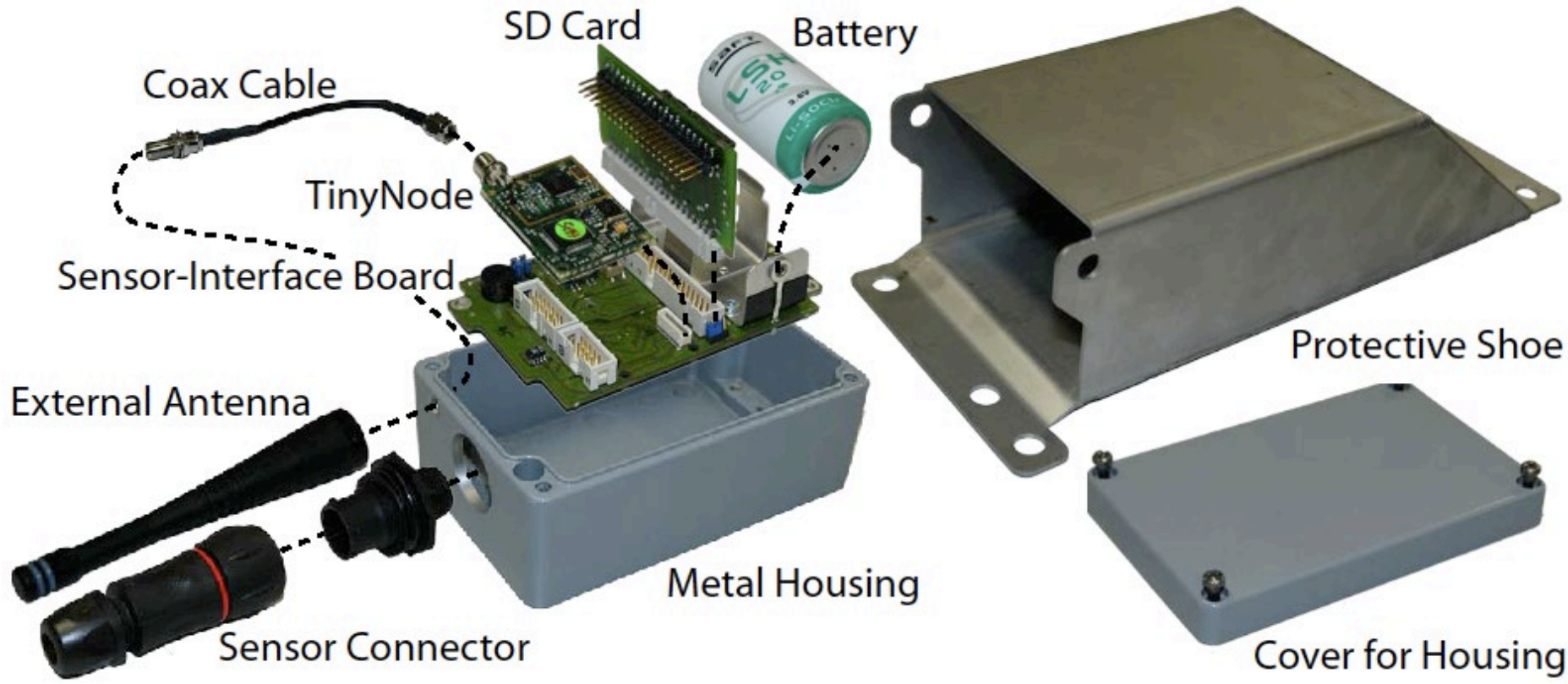




Miniature Low-Power Wireless Sensors

- Static, low-rate sensing (120 sec)
- Simple scalar values: voltages, resistivity, digital sensors
- 4-5 years operation (~150 µA avg. power)
- ~0.1 Mbyte/node/day
- 8+ years experience, ~1’276’035’519 data points

Ruggedized for Alpine Extremes



[A. Hasler et al: *Wireless Sensor Networks in Permafrost Research - Concept, Requirements, Implementation and Challenges.* Proc. 9th International Conference on Permafrost (NICOP), 2008.]

A base station collects and relays the data to the valley

[B. Buchli, F. Sutton, J. Beutel and L. Thiele: *Dynamic Power Management for Long-Term Energy Neutral Operation of Solar Energy Harvesting Systems.* Proc. SenSys 2014.

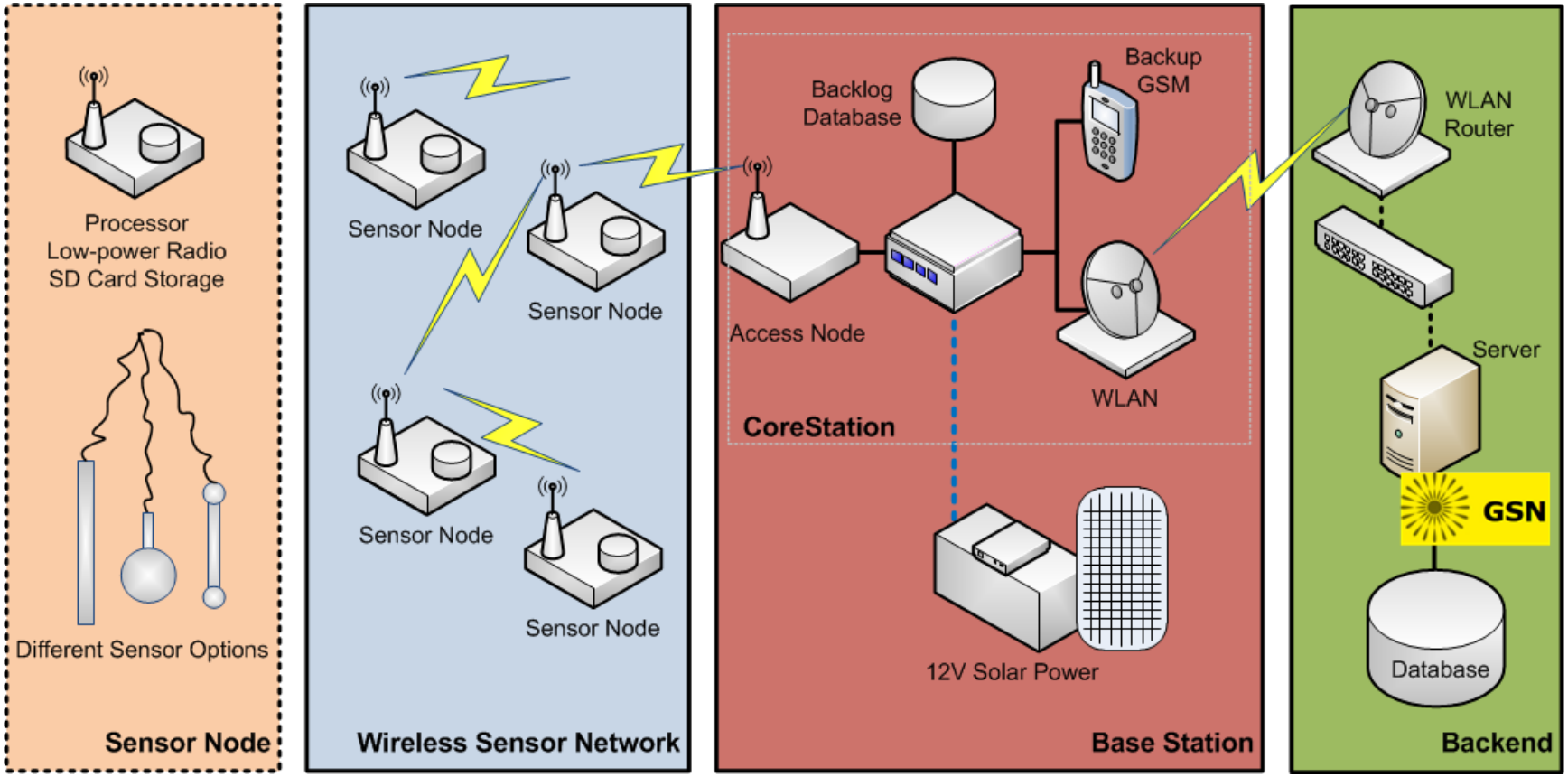
B. Buchli, F. Sutton, J. Beutel and L. Thiele: *Towards Enabling Uninterrupted Long-Term Operation of Solar Energy Harvesting Embedded Systems.* Proc. EWSN 2014

M. Keller, J. Beutel and L. Thiele: *The Problem Bit.* Proc. DCOSS 2013 ★ Best Paper Award ★

B. Buchli, D. Aschwanden and J. Beutel: Battery State-of-Charge Approximation for Energy Harvesting Embedded Systems. Proc. EWSN 2013.

M. Keller, J. Beutel and L. Thiele: *How Was Your Journey? Uncovering Routing Dynamics in Deployed Sensor Networks with Multi-hop Network Tomography.* Proc. SenSys 2012.]

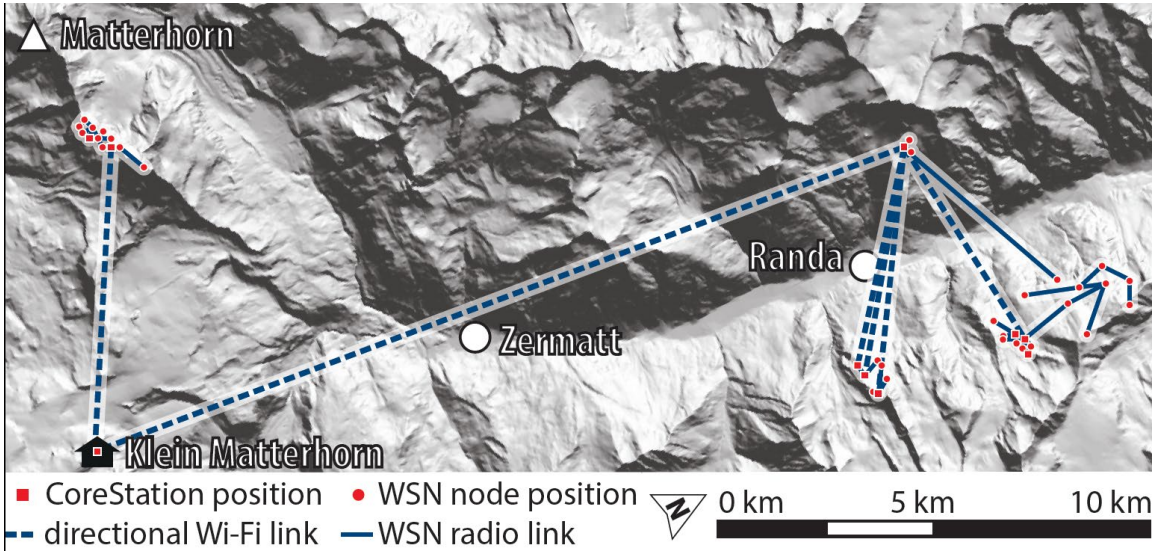
PermaSense Core System Architecture

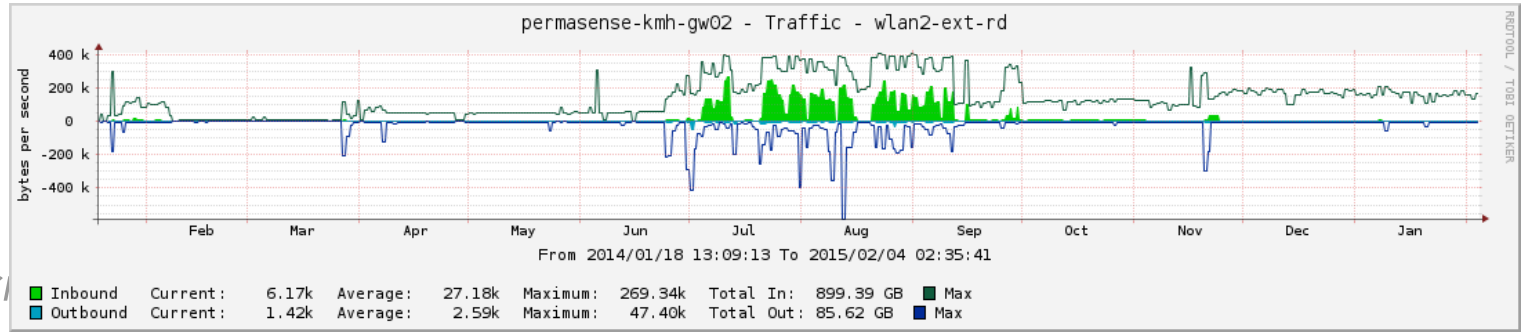


[J. Beutel et al: *PermaDAQ: A Scientific Instrument for Precision Sensing and Data Recovery under Extreme Conditions*. Proc. IPSN/SPOTS 2009.]

WLAN Long-haul Communication

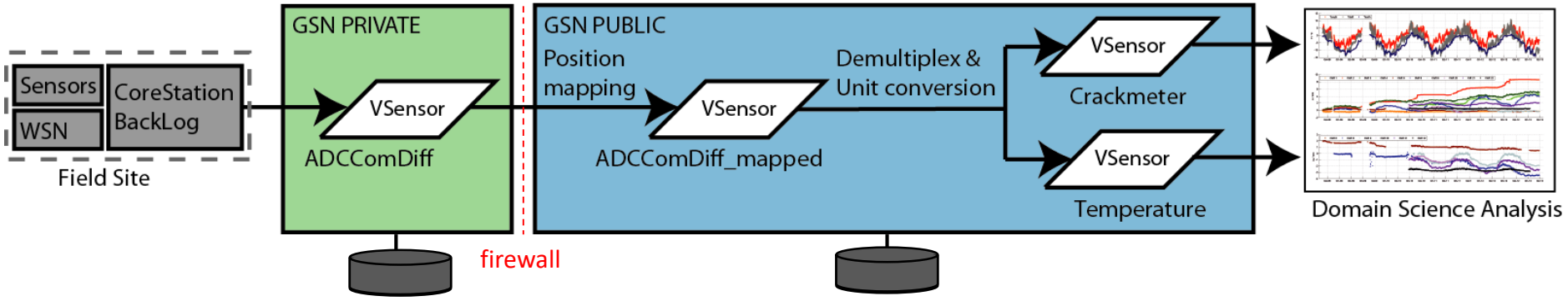
- WLAN (802.11a) backbone using directional links
- Leased fiber/DSL from Zermatt Bergbahnen AG to mountaintop





Online Data Management & Access

- Global Sensor Network (GSN)
  - Data streaming framework from EPFL (K. Aberer)
  - Organized in “virtual sensors”, i.e. data types/semantics
  - Hierarchies and concatenation of virtual sensors enable on-line processing
  - Dual architecture translates data from machine representation to SI values, adds metadata



Data from field site is received by the private GSN server “as is” and **stored** in a primary database.

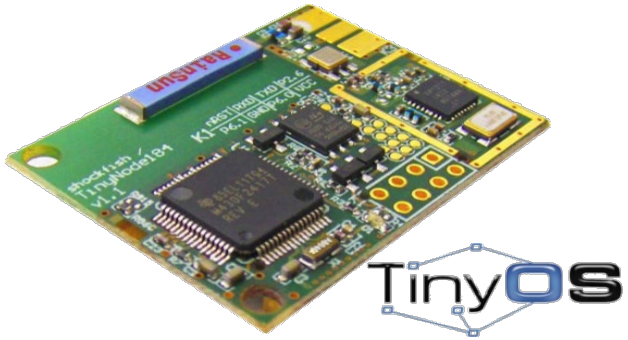
Data is passed on to a public GSN server where it is **mapped** to metadata (positions, sensor types, calibration) and **converted** to convenient data formats.

Data is available for download and analysis using **external tools**.

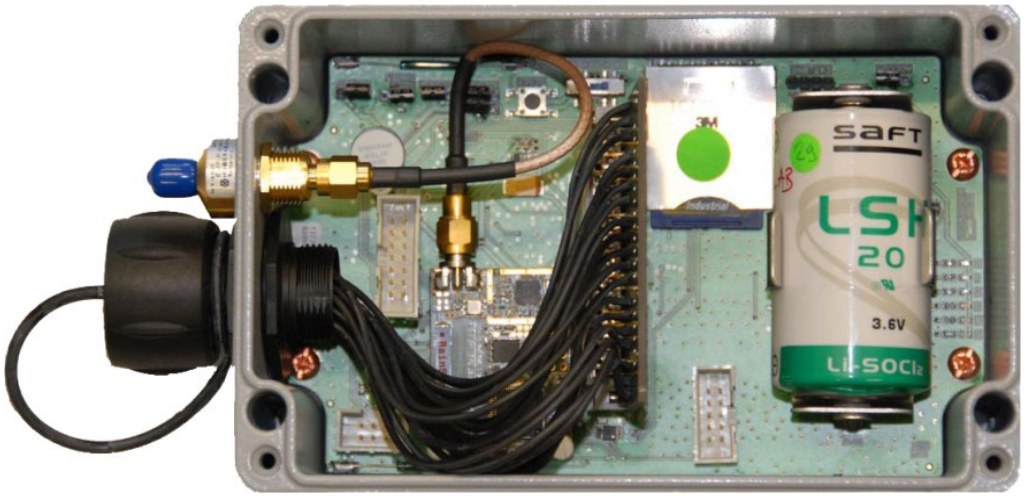
OPPORTUNITIES FOR NETWORKED EMBEDDED SYSTEMS RESEARCH

Sensor Node Hardware

- Shockfish TinyNode184
  - MSP430, 16-bit, 8MHz, 8k SRAM, 92k Flash
  - LP Radio: SX1211 @ 868 MHz



- Waterproof housing and connectors
- Sensor interface board
  - Interfaces, power control
  - Temp/humidity monitor
  - 1 GB Flash memory



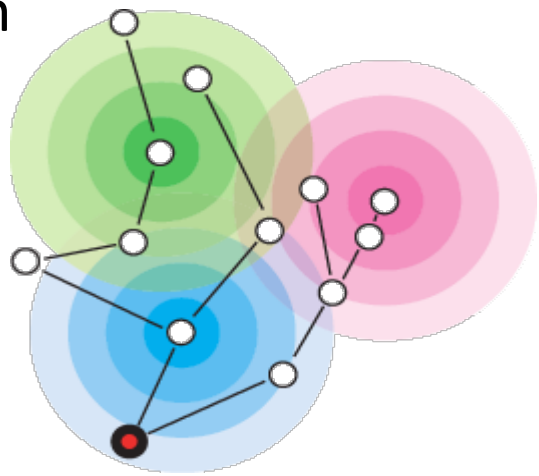
- 3-year life-time
  - Single Li-$SOCl_2$ battery, 13 Ah
  - ~300 μA power budget

[J. Beutel et al: *PermaDAQ: A Scientific Instrument for Precision Sensing and Data Recovery under Extreme Conditions*. Proc. IPSN/SPOTS 2009.]

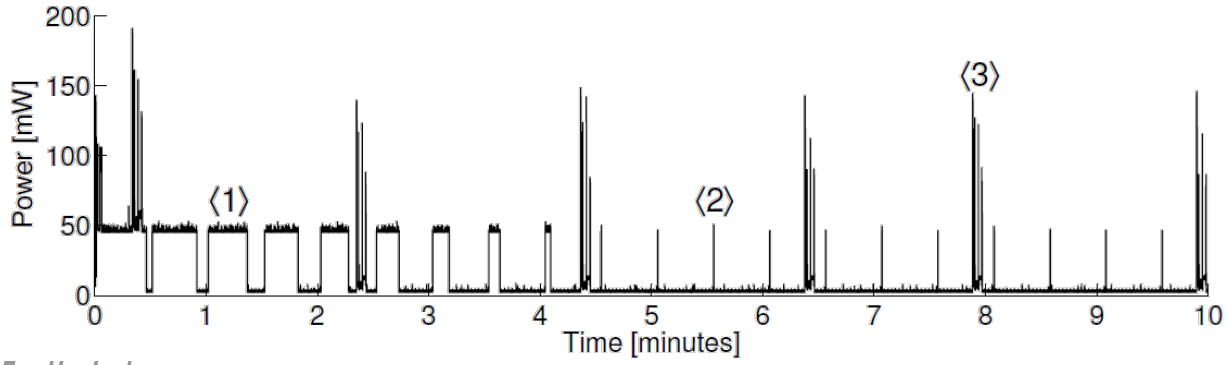
Ultra Low-Power Data Gathering

- Dozer ultra low-power data gathering system
  - Beacon based, 1-hop synchronized TDMA
  - Optimized for ultra-low duty cycles
  - **0.167%** duty-cycle, **0.032mA** (@ 30sec beacons)

- Dynamic adaptation
  - Back off randomization for diversity
  - Jitter adaptation over multiple hops
  - Account for long-term loss of connectivity



[Burri, N., von Rickenbach, P., & Wattenhofer, R.: *Dozer: Ultra-Low Power Data Gathering in Sensor Networks.* Proc. IPSN 2007.]

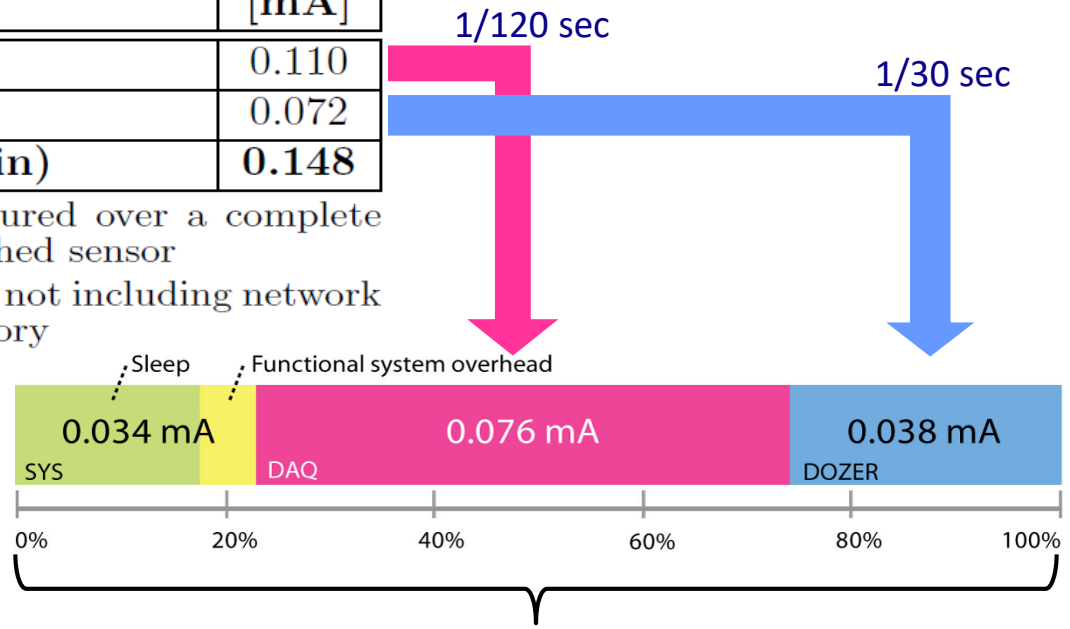


SIB: Total Power Performance Analysis

Operating Mode Characterization	[mA]
Sleep	0.026
DAQ active[a]	2.086
Dozer RX idle	13.64
Dozer RX	14.2
Dozer TX	54.6
Measured Average Values	**[mA]**
DAQ only (2min)	0.110
Dozer only (30sec/2min)[b]	0.072
PermaDozer total (30sec/2min)	**0.148**

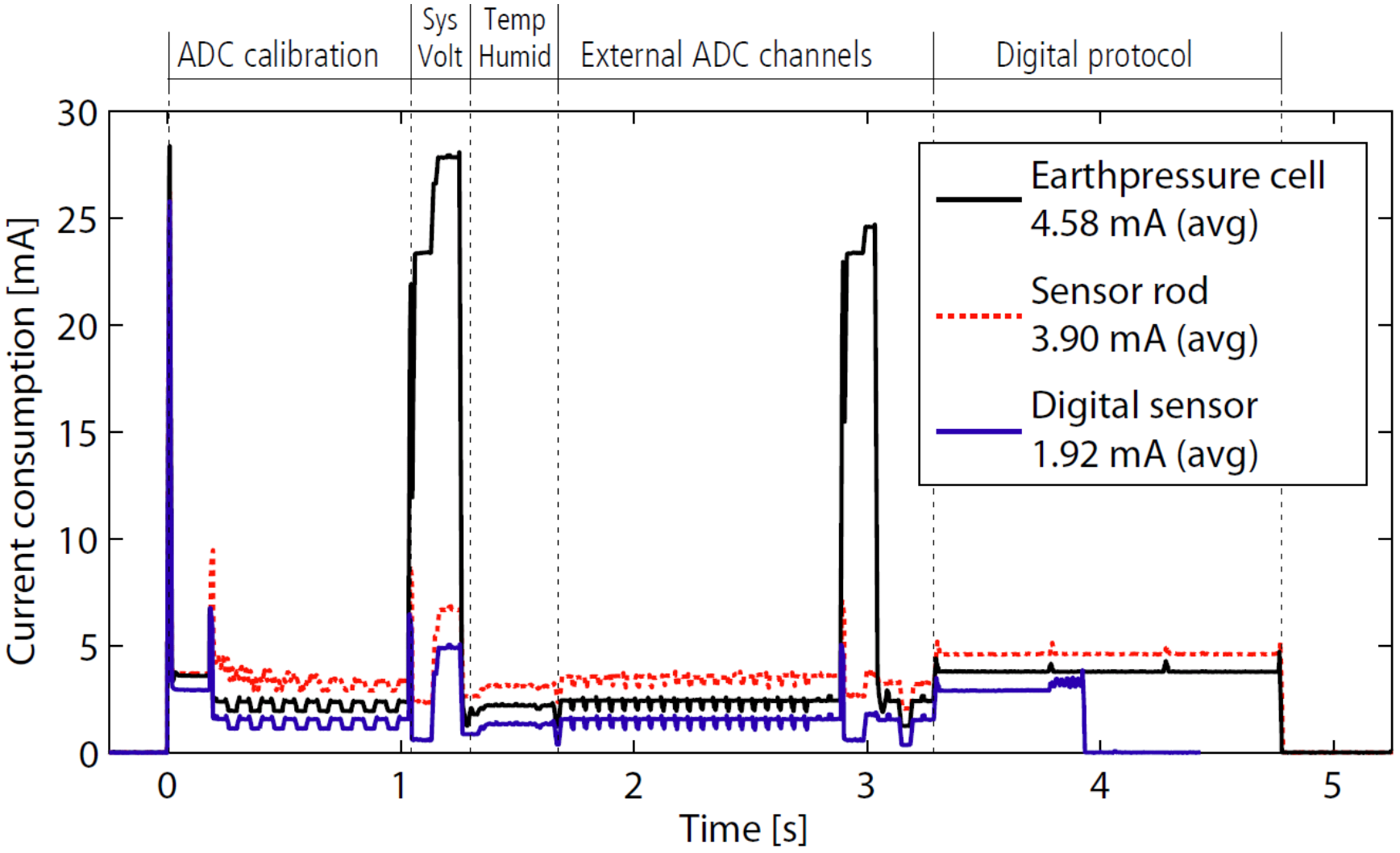
[a] Averages power consumption measured over a complete DAQ routine execution without attached sensor

[b] Dozer only includes communication, not including network initialization and access to flash memory

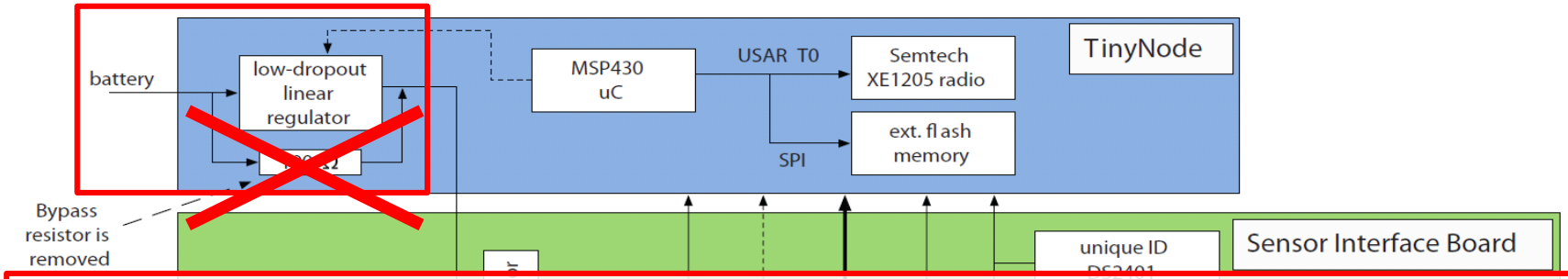


148 uA average power

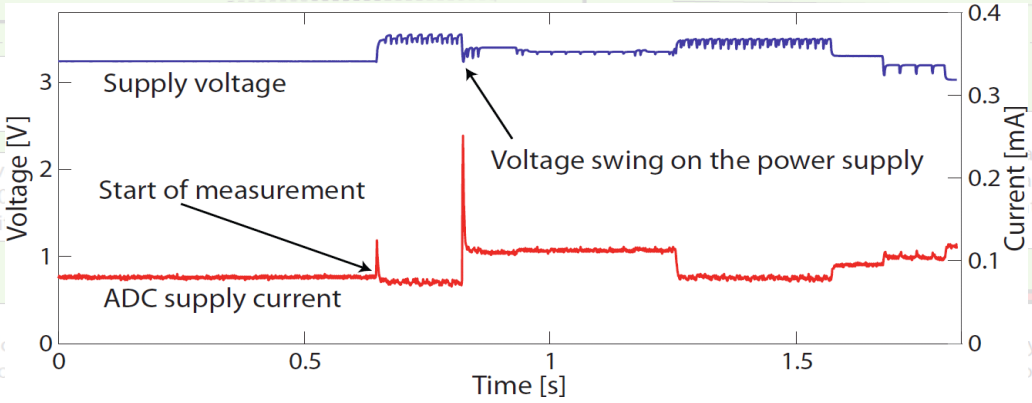
Sensors Contribute to Power Consumption



TinyNode Power Optimization – Squeeze with Implications

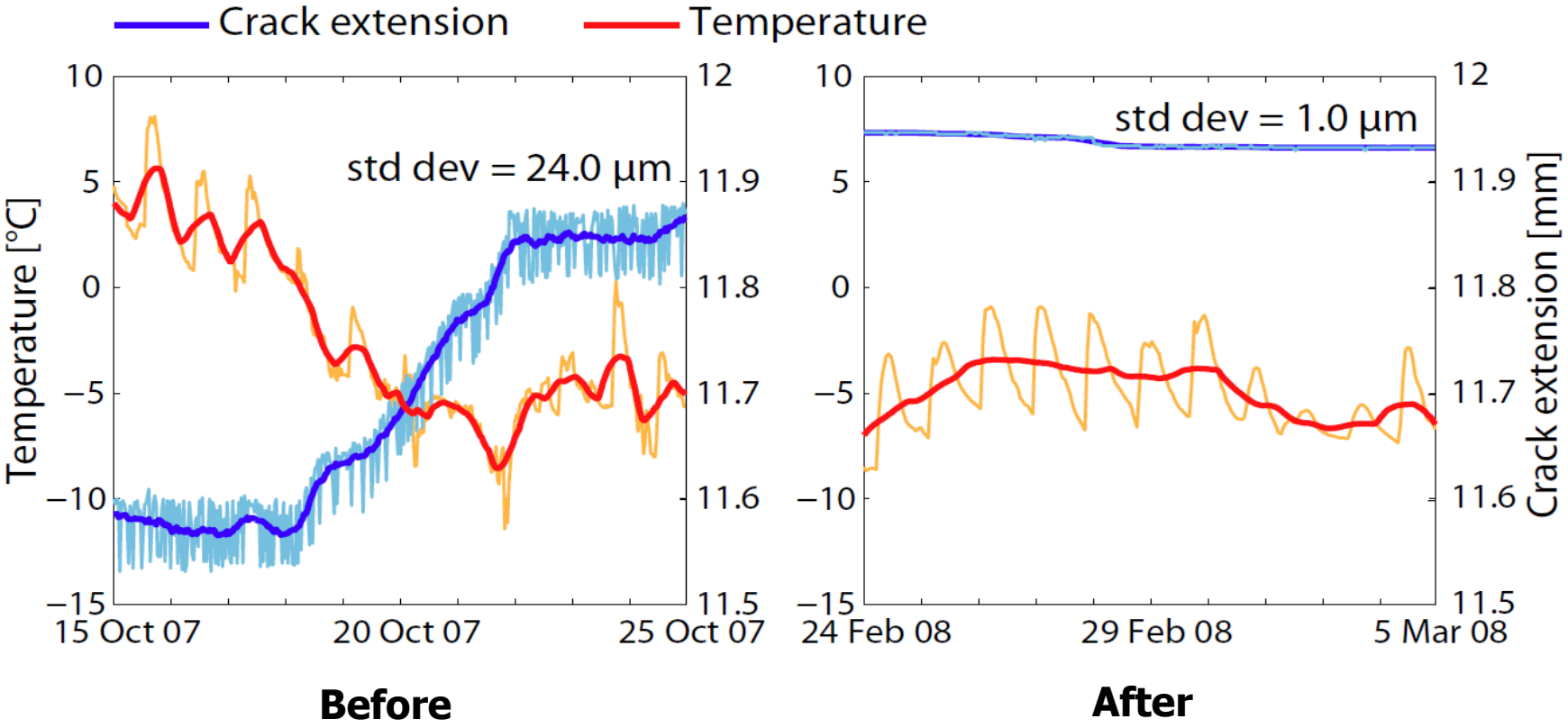


- Regulator uses 17uA quiescent current
- Bypass used to shutdown regulator -> ~1uA in standby



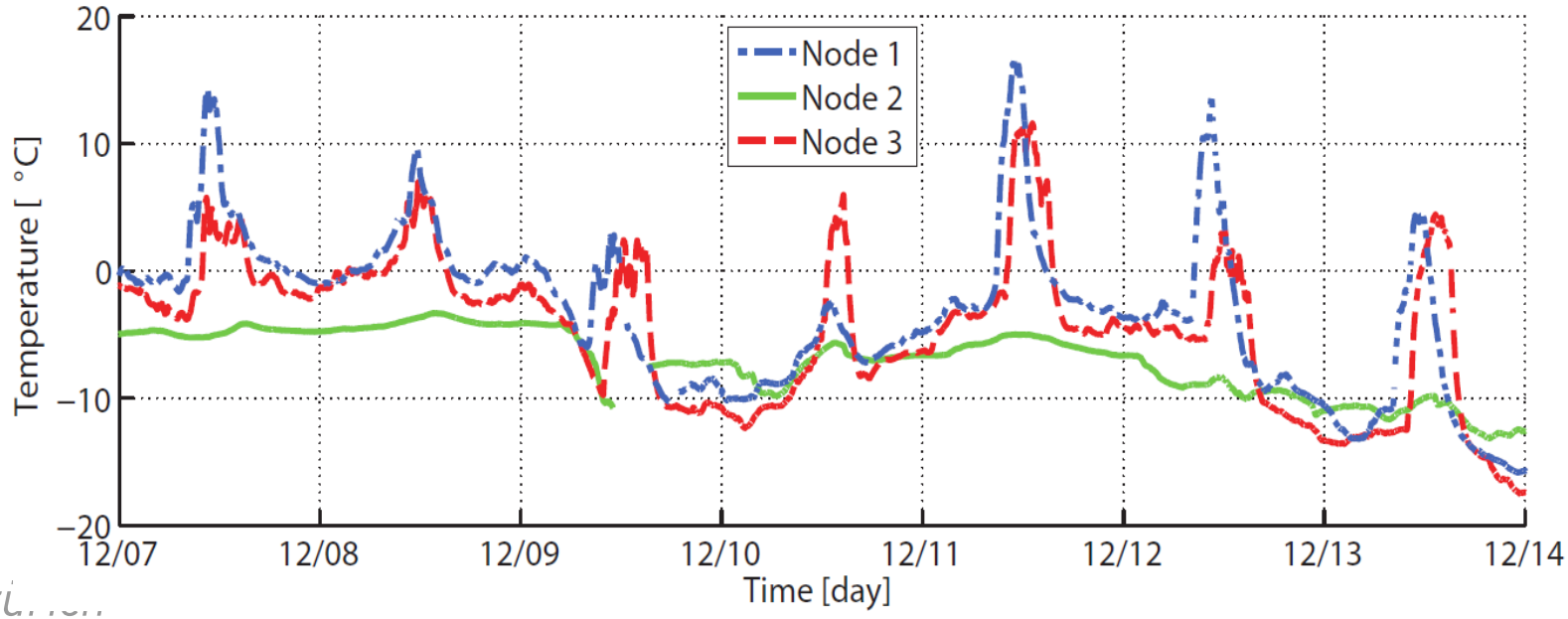
- No Bypass increases ADC accuracy: stddev 0.8844 -> 0.0706

Power Quality Increases Data Accuracy



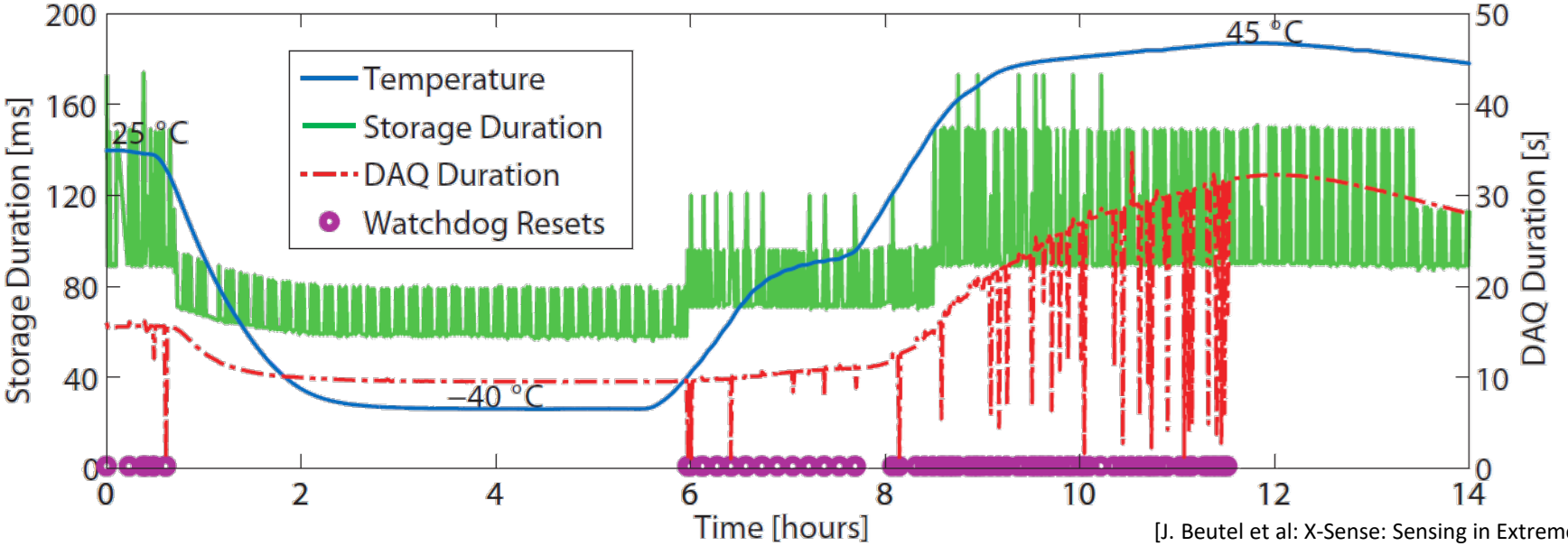
Challenge: The Physical Environment

- Strong daily variation of temperature
  - −30°C to +40°C
  - $\Delta T \leqq 20°C$/hour
- Impact on
  - timing, energy availability, fatigue, **SOFTWARE,** …



Impact of Environmental Extremes

- Tighter guard times increase energy efficiency
- Software testing in a climate chamber
  - Clock drift compensation yields ± 5ppm
- Validation of correct function



[J. Beutel et al: X-Sense: Sensing in Extreme Environments. Proc. Design, Automation and Test in Europe (DATE 2011).]

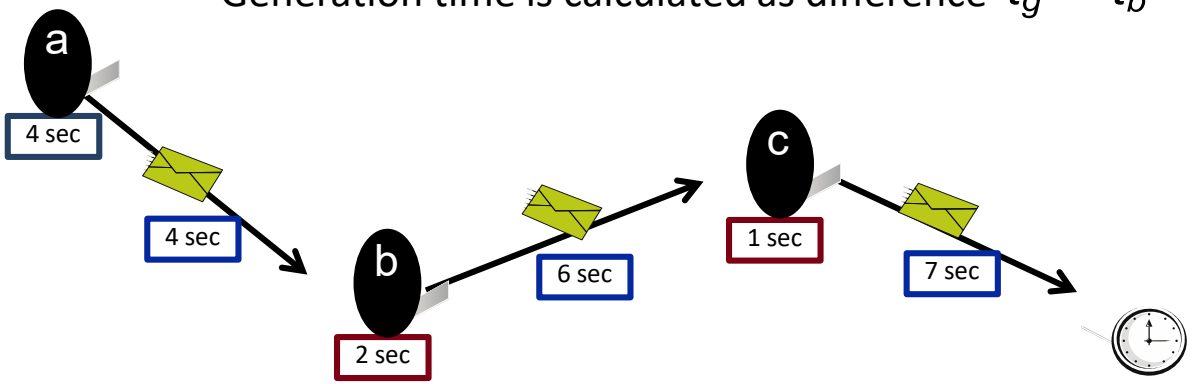
Global vs. Local Time Sync

- In cases where no network-wide time synchronization is available
  - Global time sync not available for network protocol control
  - Implications on data usage

- Solution: Elapsed time on arrival
  - Sensor nodes measure/accumulate packet sojourn time
  - Base station annotates packets with UTC timestamps
  - Generation time is calculated as difference $\tilde{t}_g = t_b - \tilde{t}_s$

[M. Keller, J. Beutel and L. Thiele: *Multi-hop network tomography: path reconstruction and per-hop arrival time estimation from partial information.* ACM SIGMETRICS Performance Evaluation Review Volume 40, Issue 1, p. 421-422, 2012.

M. Keller, J. Beutel and L. Thiele: *How Was Your Journey? Uncovering Routing Dynamics in Deployed Sensor Networks with Multi-hop Network Tomography.* Proc. SenSys 2012.]



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Today's Hot Researcher & Paper

- Margaret Martonosi
  - Faculty at Princeton
- Computer architecture and mobile computing with a particular focus on power-efficiency.
  - Wattch power modeling infrastructure
- IEEE and ACM Fellow
  - "For contributions in power-aware computing"

David Brooks, Vivek Tiwari, and Margaret Martonosi (2000). *Wattch: a framework for architectural-level power analysis and optimizations*. 27th Annual International Symposium on Computer Architecture (ISCA '00).: p. 83–94.

Recap of Today

- **Modern embedded hardware** (equally for high performance SoCs) offer a **great feature set**
  - Many integrated peripherals/options
  - Meticulous **attention to power performance in all operating modes**

- **Software** control is **increasingly difficult**
  - Lack of support by design flow/tools
  - Overall system complexity

- **Profiling methods necessary** to assess system level performance
  - Detailed figures in documentations work only for each unique case
  - Modeling capabilities are limited (we will discuss this in detail)