Low-Power System Design

227-0781-00L

Fall Semester 2019

Jan Beutel

Plan for Today

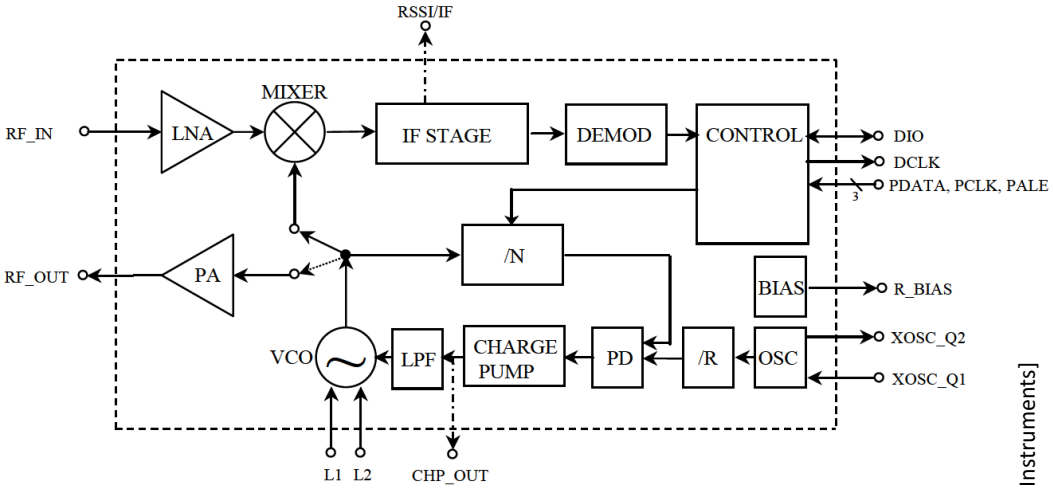
- LP system architectures – processor and radio systems
- Platform metrics
- Current Research Example
  - Managing Concurrency on the Dual-Processor Platform

Low-Power System Design

LOW-POWER RADIO SUBSYSTEMS

Basic Radio Architecture: CC1000

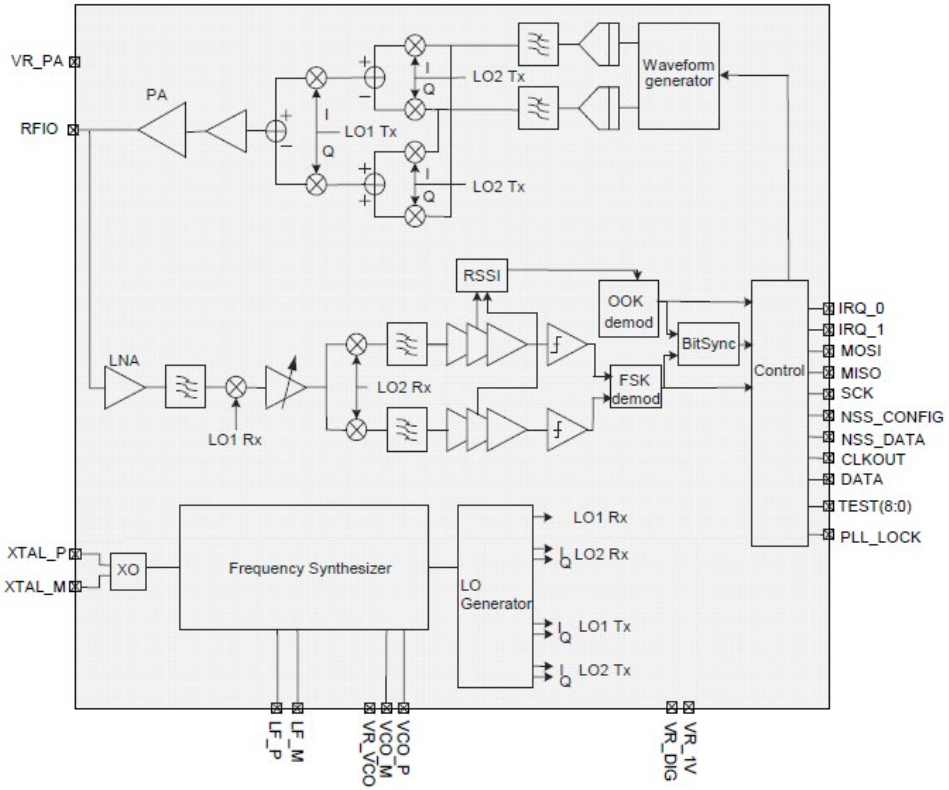
- Separate RX and TX modes (half-duplex)
  - Switching time between RX/TX
- Receive mode
  - Traditional superheterodyne receiver feeding a demodulator (DEMOD)
  - RSSI signal (or the IF signal after the mixer) is available at the RSSI/IF
  - Digital demodulated data on the pin DIO
  - On-chip synchronization of data
- Transmit mode
  - Frequency shift keying (FSK) of digital bit stream (DIO)
  - Voltage controlled oscillator (VCO) signal fed directly to power amplifier (PA)
- Simple global power-domain



[Texas Instruments]

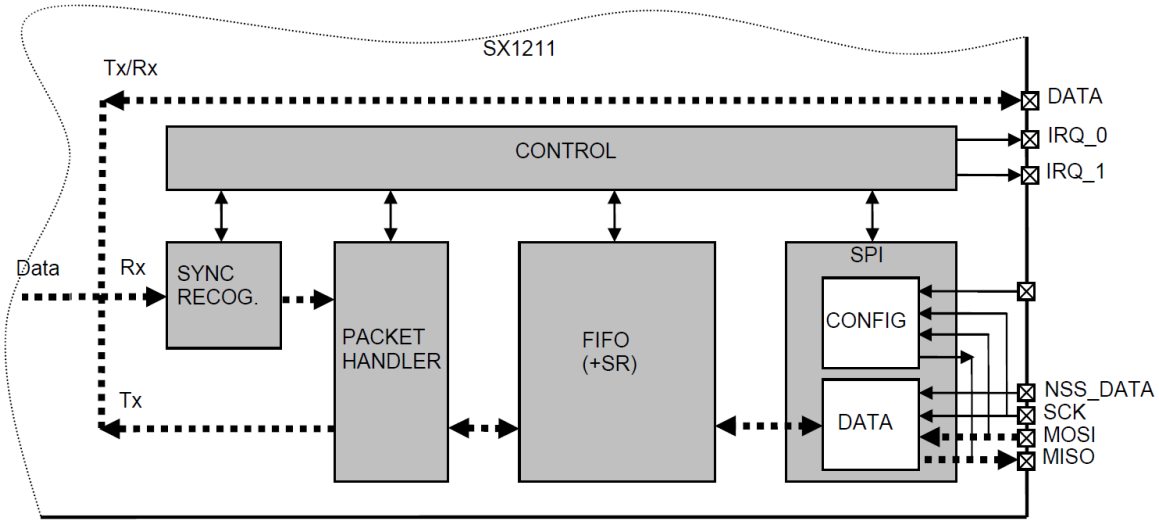
Adding Buffering/Packet Data: SX1211

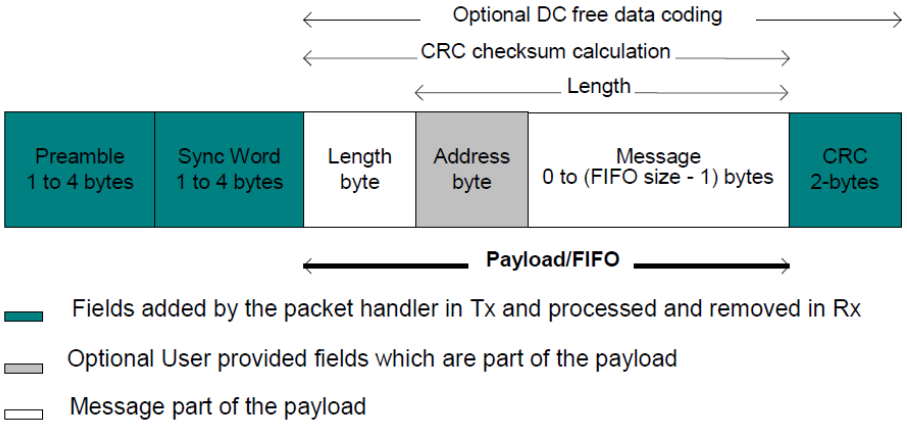
- **T**hree different data operation modes
- Continuous mode
  - Each bit is accessed in real time at DATA
  - Requires adequate external signal processing
- Buffered mode
  - Byte-level interface with FIFO
  - Reduced uC overhead
  - Unlimited packet length
- Packet mode (recommended)
  - Packet is automatically built with preamble, sync word, and optional CRC
  - User only provides/retrieves payload bytes to/from FIFO
  - Maximum payload length is limited to the maximum FIFO limit of 64 bytes



[Semtech]

Simple Packet Interface: SX2111

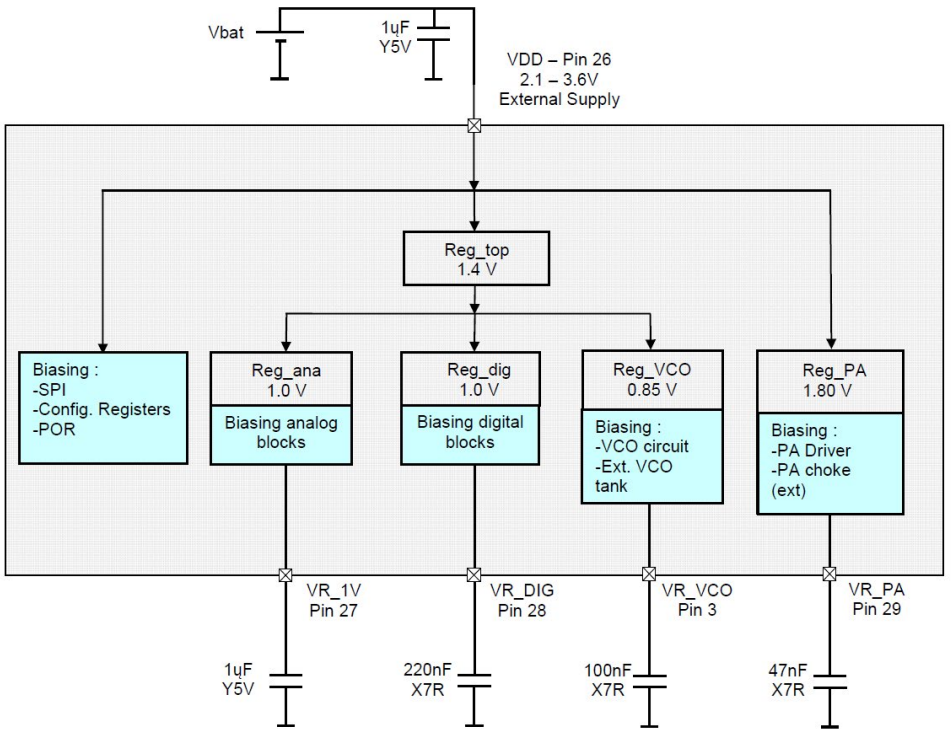




[Semtech]

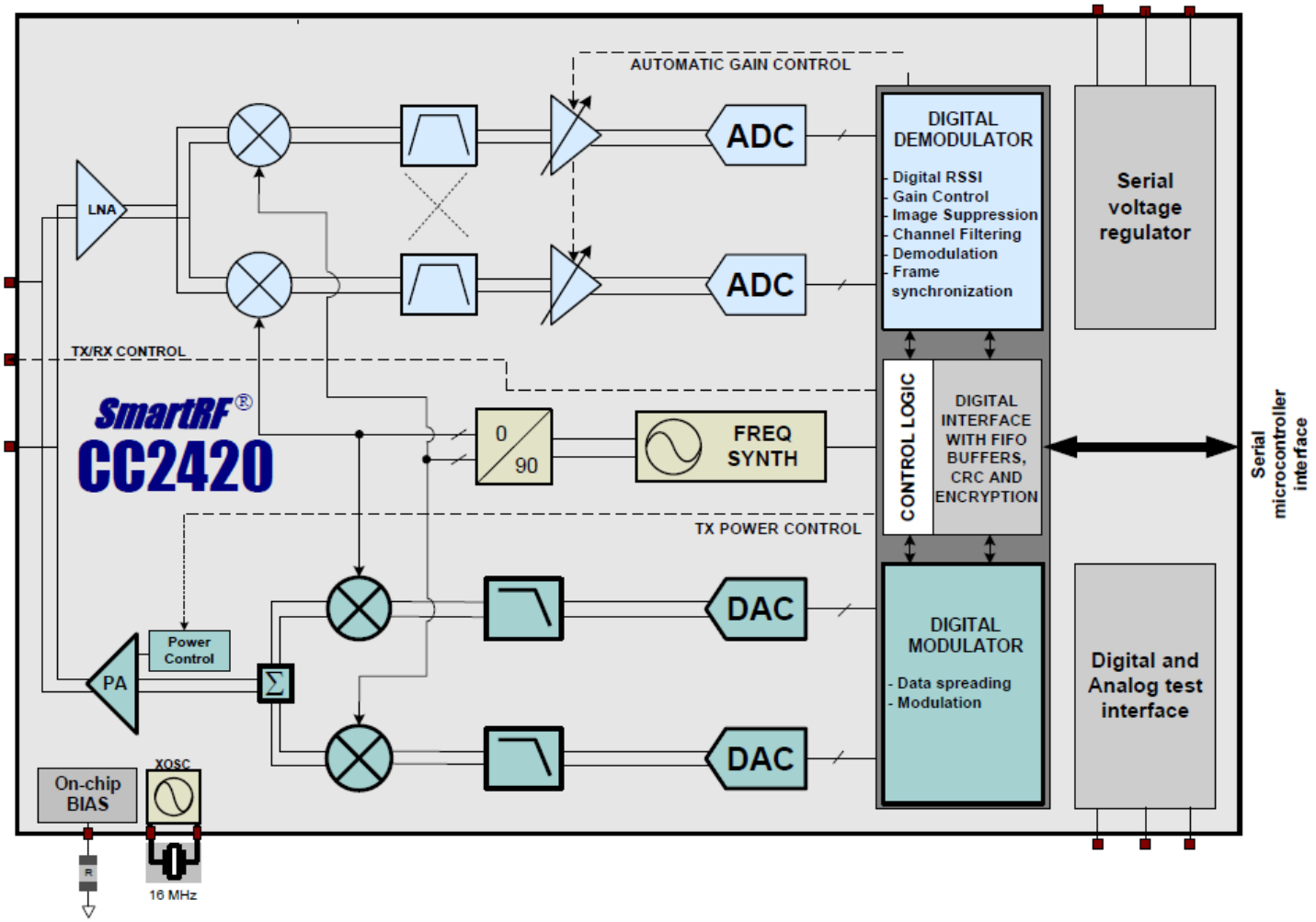
Multi-Level Internal Power Control

- Global power control
  - Internal precision voltage regulator
  - Lower core voltage
  - Lower noise supply
  - Separation of concerns
- Per-domain power control
  - Separate regulation/control of subsystems
  - Variable power footprint
  - Increased flexibility
- In reality
  - Not all options can be leveraged
  - One operating scheme chosen at design time



[Semtech]

Integrated Protocol Processing: CC2420



[Texas Instruments]

CC2420 Power Control

- Internal LDO with external control
  - Registers and RAM are lost on disable (leakage current drops beyond retention)
  - Reset required on disable/re-enable
  - Significant setup time for radio

- Battery Monitor
  - Enables monitoring the unregulated voltage input
  - Programmable threshold
  - Will not work when the voltage regulator is not used
  - Information given as status bit

6.8 Voltage Regulator

Parameter	Min.	Typ.	Max.	Unit	Condition / Note
General					Note that the internal voltage regulator can only supply CC2420 and no external circuitry.
Input Voltage	2.1	3.0	3.6	V	On the VREG_IN pin
Output Voltage	1.7	1.8	1.9	V	On the VREG_OUT pin
Quiescent current	13	20	29	µA	No current drawn from the VREG_OUT pin. Min and max numbers include 2.1 through 3.6 V input voltage
Start-up time		0.3	0.6	ms	

6.9 Battery Monitor

Parameter	Min.	Typ.	Max.	Unit	Condition / Note
Current consumption	6	30	90	µA	When enabled
Start-up time			100	µs	Voltage regulator already enabled
Settling time			2	µs	New toggle voltage programmed

[Texas Instruments]

CC2420 Power Modes

6.10 Power Supply

Parameter	Min.	Typ.	Max.	Unit	Condition / Note
Current consumption in different modes (see Figure 25, page 44)					Current drawn from VREG_IN, through voltage regulator
Voltage regulator off (OFF) Power Down mode (PD) Idle mode (IDLE)		0.02 20 426	1	µA µA µA	Voltage regulator off Voltage regulator on Including crystal oscillator and voltage regulator
Current Consumption, receive mode		18.8		mA	

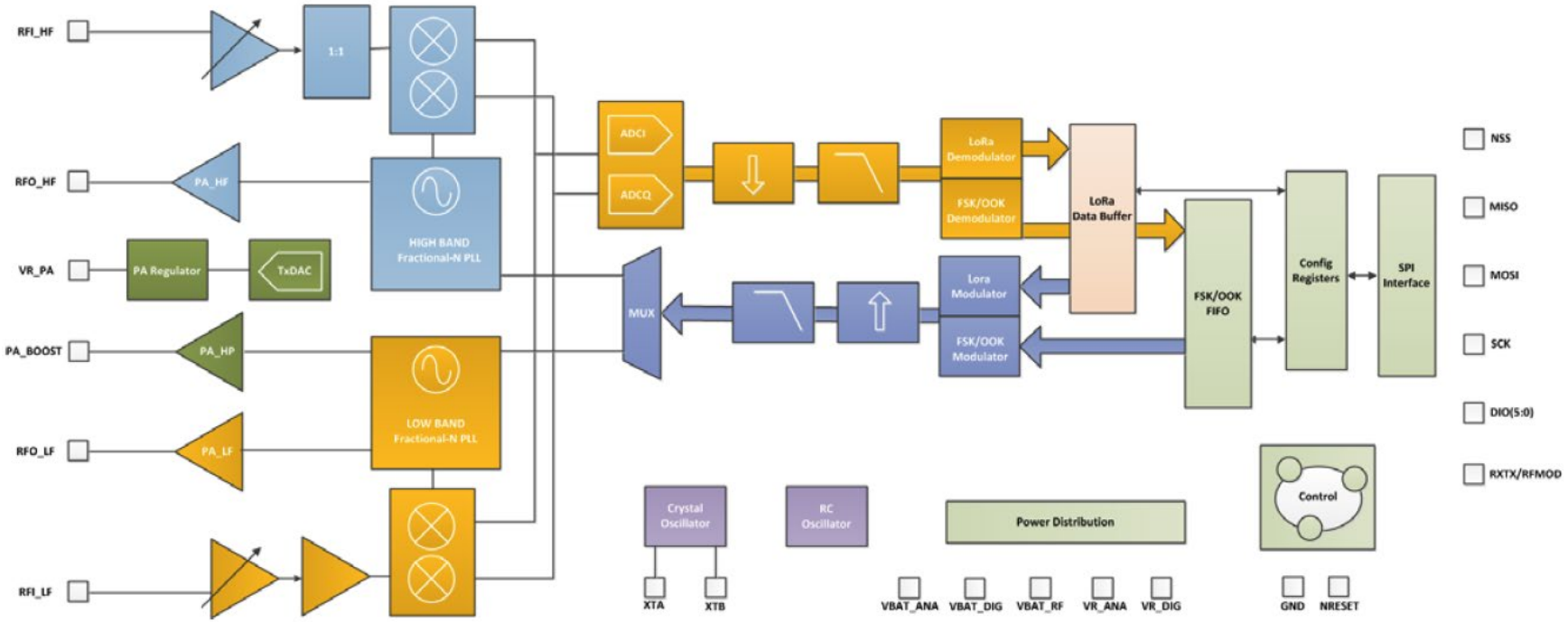
Parameter	Min.	Typ.	Max.	Unit	Condition / Note
Current Consumption, transmit mode:					
P = -25 dBm P = -15 dBm P = -10 dBm P = −5 dBm P = 0 dBm		8.5 9.9 11 14 17.4		mA mA mA mA mA	The output power is delivered differentially to a 50 Ω singled ended load through a balun, see also page 54.

[Texas Instruments]

CC430F513x MSP430™ SoC With RF Core

- True System-on-Chip (SoC) for Low-Power Wireless Communication Applications
- Wide Supply Voltage Range: 3.6 V Down to 1.8 V
- Ultra-Low Power Consumption
  - CPU Active Mode (AM): 160 µA/MHz
  - Standby Mode (LPM3 RTC Mode): 2.0 µA
  - Off Mode (LPM4 RAM Retention): 1.0 µA
  - Radio in RX: 15 mA, 250 kbps, 915 MHz
- MSP430™ System and Peripherals
  - 16-Bit RISC Architecture, Extended Memory, up to 20-MHz System Clock
  - Wake up From Standby Mode in Less Than 6 µs
  - Flexible Power-Management System With SVS and Brownout
  - Unified Clock System With FLL
  - 16-Bit Timer TA0, Timer_A With Five Capture/Compare Registers
  - 16-Bit Timer TA1, Timer_A With Three Capture/Compare Registers
  - Hardware Real-Time Clock (RTC)
  - Two Universal Serial Communication Interfaces (USCIs)
    - USCI_A0 Supports UART, IrDA, SPI
    - USCI_B0 Supports I^2C, SPI
  - 12-Bit Analog-to-Digital Converter (ADC) With Internal Reference, Sample-and-Hold, and Autoscan Features (CC430F613x and CC430F513x Only)
  - Comparator
  - Integrated LCD Driver With Contrast Control for up to 96 Segments (Only CC430F61xx)
  - 128-Bit AES Security Encryption and Decryption Coprocessor
  - 32-Bit Hardware Multiplier
  - 3-Channel Internal DMA
  - Serial Onboard Programming, No External Programming Voltage Needed
  - Embedded Emulation Module (EEM)
- High-Performance Sub-1 GHz RF Transceiver Core
  - Same as in CC1101
  - Wide Supply Voltage Range: 2 V to 3.6 V
  - Frequency Bands: 300 MHz to 348 MHz, 389 MHz to 464 MHz, and 779 MHz to 928 MHz
  - Programmable Data Rate From 0.6 kBaud to 500 kBaud
  - High Sensitivity (–117 dBm at 0.6 kBaud, –111 dBm at 1.2 kBaud, 315 MHz, 1% Packet Error Rate)
  - Excellent Receiver Selectivity and Blocking Performance
  - Programmable Output Power up to +12 dBm for All Supported Frequencies
  - 2-FSK, 2-GFSK, and MSK Supported, Also OOK and Flexible ASK Shaping
  - Flexible Support for Packet-Oriented Systems: On-Chip Support for Sync Word Detection, Address Check, Flexible Packet Length, and Automatic CRC Handling
  - Support for Automatic Clear Channel Assessment (CCA) Before Transmitting (for Listen-Before-Talk Systems)
  - Digital RSSI Output
  - Suited for Systems Targeting Compliance With EN 300 220 (Europe) and FCC CFR Part 15 (US)
  - Suited for Systems Targeting Compliance With Wireless M-Bus Standard EN 13757-4:2005
  - Support for Asynchronous and Synchronous Serial Receive or Transmit Mode for Backward Compatibility With Existing Radio Communication Protocols
- Device Comparison Summarizes the Available Family Members

New LoRa Transceivers – SX127x



Part Number	Frequency Range	Spreading Factor	Bandwidth	Effective Bitrate	Est. Sensitivity
SX1276	137 - 1020 MHz	6 - 12	7.8 - 500 kHz	.018 - 37.5 kbps	-111 to -148 dBm
SX1277	137 - 1020 MHz	6 - 9	7.8 - 500 kHz	0.11 - 37.5 kbps	-111 to -139 dBm
SX1278	137 - 525 MHz	6- 12	7.8 - 500 kHz	.018 - 37.5 kbps	-111 to -148 dBm
SX1279	137 - 960MHz	6- 12	7.8 - 500 kHz	.018 - 37.5 kbps	-111 to -148 dBm

[Semtech]

New LoRa Transceivers – SX127x

GENERAL DESCRIPTION

The SX1272/73 transceivers feature the LoRa™ long range modem that provides ultra-long range spread spectrum communication and high interference immunity whilst minimising current consumption.

Using Semtech's patented LoRa™ modulation technique SX1272/73 can achieve a sensitivity of over -137 dBm using a low cost crystal and bill of materials. The high sensitivity combined with the integrated +20 dBm power amplifier yields industry leading link budget making it optimal for any application requiring range or robustness. LoRa™ also provides significant advantages in both blocking and selectivity over conventional modulation techniques, solving the traditional design compromise between range, interference immunity and energy consumption.

These devices also support high performance (G)FSK modes for systems including WMBus, IEEE802.15.4g. The SX1272/73 deliver exceptional phase noise, selectivity, receiver linearity and IIP3 for significantly lower current consumption than competing devices.

ORDERING INFORMATION

KEY PRODUCT FEATURES

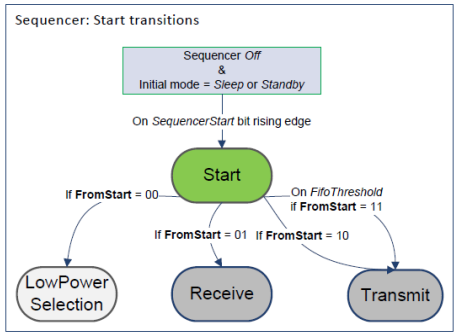
- LoRa™ Modem
- 157 dB maximum link budget
- +20 dBm at 100 mW constant RF output vs. V supply
- +14 dBm high efficiency PA
- Programmable bit rate up to 300 kbps
- High sensitivity: down to -137 dBm
- Bullet-proof front end: IIP3 = -12.5 dBm
- 89 dB blocking immunity
- Low RX current of 10 mA, 100 nA register retention
- Fully integrated synthesizer with a resolution of 61 Hz
- FSK, GFSK, MSK, GMSK, LoRa™ and OOK modulation
- Built-in bit synchronizer for clock recovery
- Preamble detection
- 127 dB Dynamic Range RSSI
- Automatic RF Sense and CAD with ultra-fast AFC
- Packet engine up to 256 bytes with CRC
- Built-in temperature sensor and low battery indicator

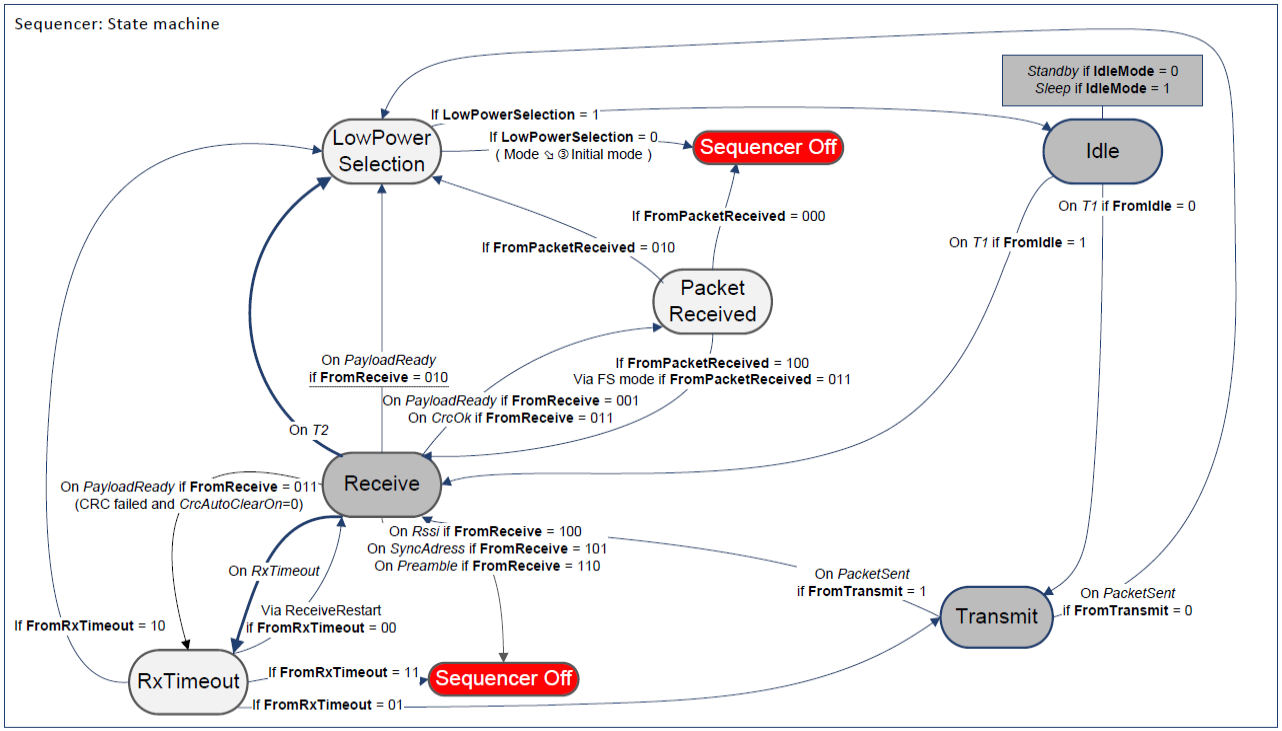
[Semtech]

Built-in Protocol State Machines

4.2.8. Top Level Sequencer

Depending on the application, it is desirable to be able to change the mode of the circuit according to a predefined sequence without access to the serial interface. In order to define different sequences or scenarios, a user-programmable state machine, called Top Level Sequencer (Sequencer in short), can automatically control the chip modes.



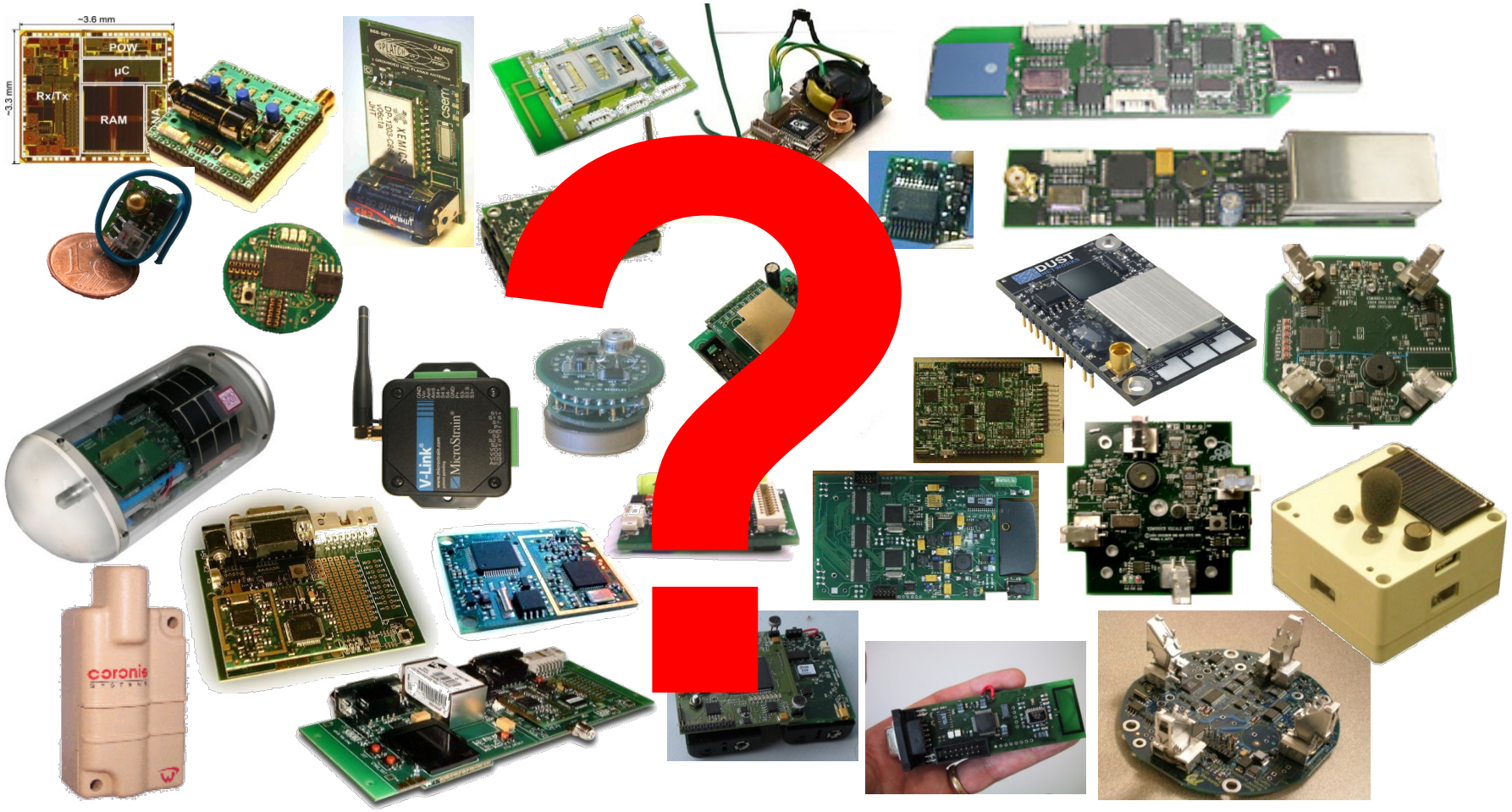


[Semtech]

Low-Power System Design

COMPARING PLATFORMS – METRICS

How To Compare Systems…



State-of-the-Art Platforms – Metrics

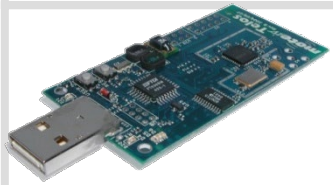
Mica2

Mica2Dot

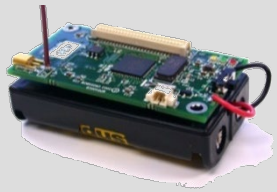
Tmote Sky

Imote

Simple Metrics – Tabular Data

 Mica2	Atmel AVR + CC1000 + 3xLED + 51pin + 2xAA + …
 Mica2Dot	Atmel AVR + CC1000 + 1xLED + 4MHz + 19pin + round + 1xCoin Cell + …
 Tmote Sky	TI MSP430 + CC2420 + 3xLED + Sensors + USB + 1Mbit Flash + …
 Imote	ARM7 + Zeevo TC2001 + 2xDuoLED + 2xCR2 + …

Tales of Tables – Datasheet Magic…



Mica2

Mica2Dot

Original Crossbow Mica2 and Mics2Dot Datasheets

Processor/Radio Board	MPR500CA
Processor Performance	
Program Flash Memory	128K bytes
Measurement (Serial) Flash	512K bytes
Configuration EEPROM	4K bytes
Serial Communications	UART
Analog to Digital Converter	10 bit ADC
Other Interfaces	DIO
Current Draw	8 mA
	< 15 µA

CPU: 7.3 MHz

Processor/Radio Board	MPR400CB
Processor Performance	
Program Flash Memory	128K bytes
Measurement (Serial) Flash	512K bytes
Configuration EEPROM	4K bytes
Serial Communications	UART
Analog to Digital Converter	10 bit ADC
Other Interfaces	DIO,I2C,SPI
Current Draw	8 mA
	< 15 µA

CPU: 4 MHz

Tales of Tables – Context and Detail…

Mote Type Year	WeC 1998	René 1999	René2 2000	Dot 2000	Mica 2001	Mica2Dot 2002	Mica 2 2002	Telos 2004
Microcontroller								
Type			ATmega163		ATmega128			TI MSP430
Progra			16		128			48
RAM (KB)			1		4			10
Active Power (mW)	15		15		8		33	3
Sleep Power (μW)	45		45		75		75	15
Wakeup Time (μs)	1000		36		180		180	6
Nonvolatile storage								
Chip	24LC256				AT45DB041B			ST M25P80

SPOTS Paper

T_A = -40°C to 85°C, V_{CC} = 2.7V to 5.5V (unless otherwise noted) (Continued)

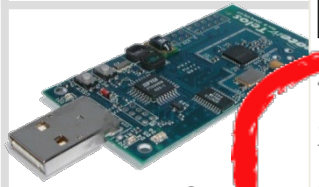
Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{CC}	Power Supply Current	Active 4 MHz, V_{CC} = 3V (ATmega128L)			5.5	mA
		Active 8 MHz, V_{CC} = 5V (ATmega128)			19	mA
		Idle 4 MHz, V_{CC} = 3V (ATmega128L)			2.5	mA
		Idle 8 MHz, V_{CC} = 5V (ATmega128)			11	mA
	Power-down mode	WDT enabled, V_{CC} = 3V		< 15	25	µA
		WDT disabled, V_{CC} = 3V		< 5	10	µA

Atmel Datasheet

Simple Metrics – Tabular Data

Mica2

Mica2Dot



Tmote Sky

Imote

Table 3-4: State of the art platform comparison – power supply and consumption

	Mica2[a]	**Mica2Dot**[a]	**Tmote Sky**[b]	**Imote**
Battery Supply	2 AA cells	1 coin cell	2 AA cells	2 CR2 cells
Minimum Vcc	2.7 V[c]	2.7 V[c]	2.1 V[d]	3.0 V
Battery Capacity	2000 mAh	560 mAh	2900 mAh	1600 mAh
Regulated Supply	–	–	–[d]	yes
CPU sleep, Radio off	0.054 mW[e]	0.054 mW[e]	0.0153 mW[e]	9 mW[f]
CPU on, Radio off	36 mW	36 mW	5.4 mW	27 mW[f]
CPU on, Radio listen[g]	66 mW	66 mW	65.4 mW	62.1 mW[f]
CPU on, Radio RX/TX	117 mW	117 mW	58.5 mW	112.5 mW[h]
Max. Power	165 mW	165 mW	69 mW	195 mW[h]

[a] Typical datasheet values. Power consumption values computed by summation of individual power consumption of system core, flash memory (Flash) memory and radio components given in datasheets at Vcc=3.0 V.

[b] Typical datasheet values as reported for the whole system. Power consumption computed at 3.0 V.

[c] Operation from rechargeable cells (Vcc=2.4 V) unreliable.

[d] The system is fed directly from batteries with a regulated power supply at 1.8 V available for the radio transceiver only. The CPU requires a minimum Vcc=2.1V.

[e] Wakeup possible from internal timer only.

[f] Power measurements on live system at Vcc=3.0 V as reported by Nachman et al. [NKA+05].

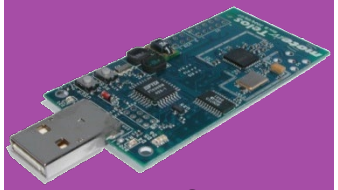
[g] Radio listening typically assumes a worst case of CPU active and radio RX at the nominal datarate.

[h] Datasheet values at Vcc=3.0 V for radio SoC only (no peripherals).

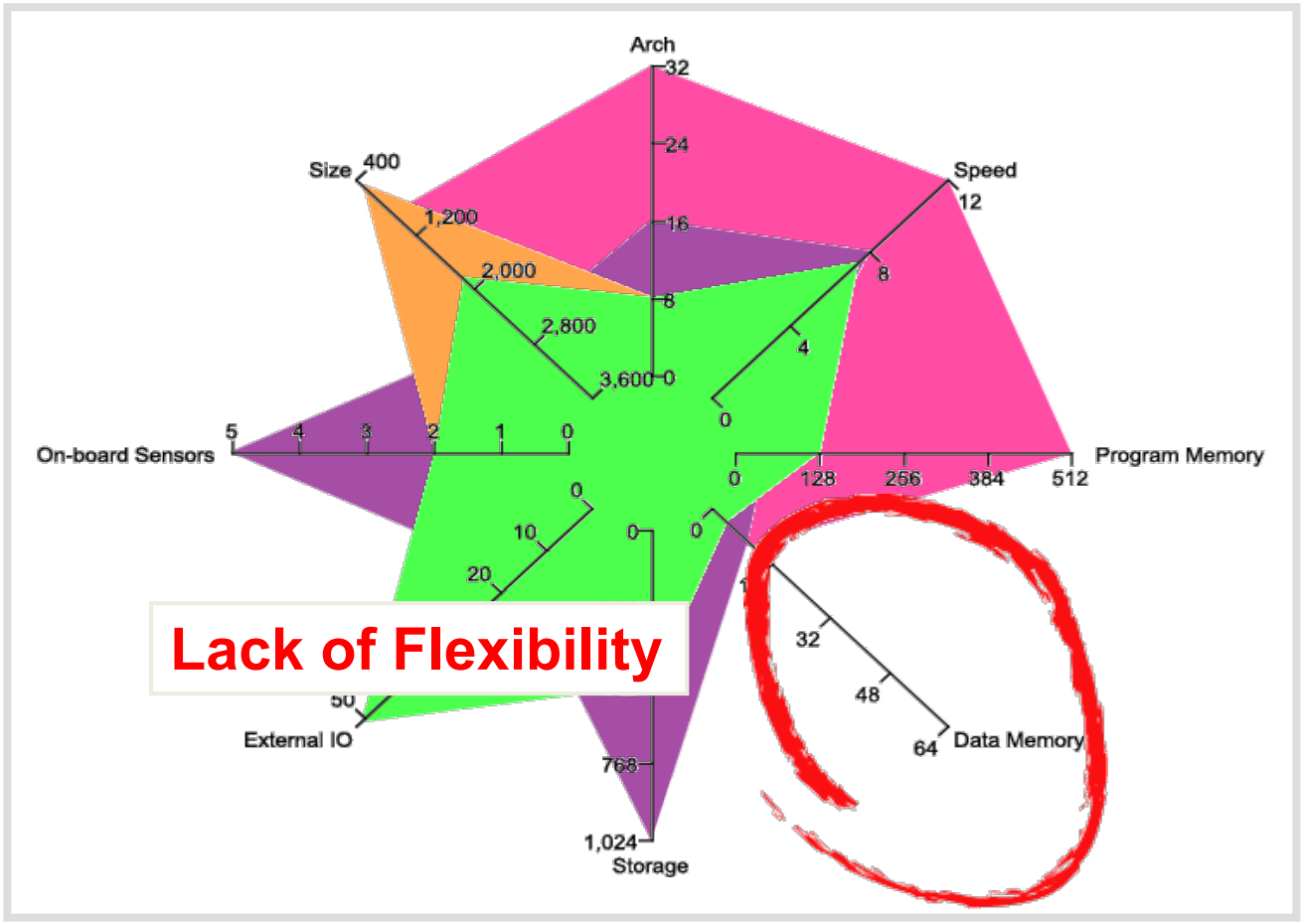
Comparing the System Core


Mica2


Mica2Dot


Tmote Sky

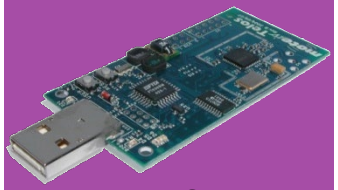

Imote



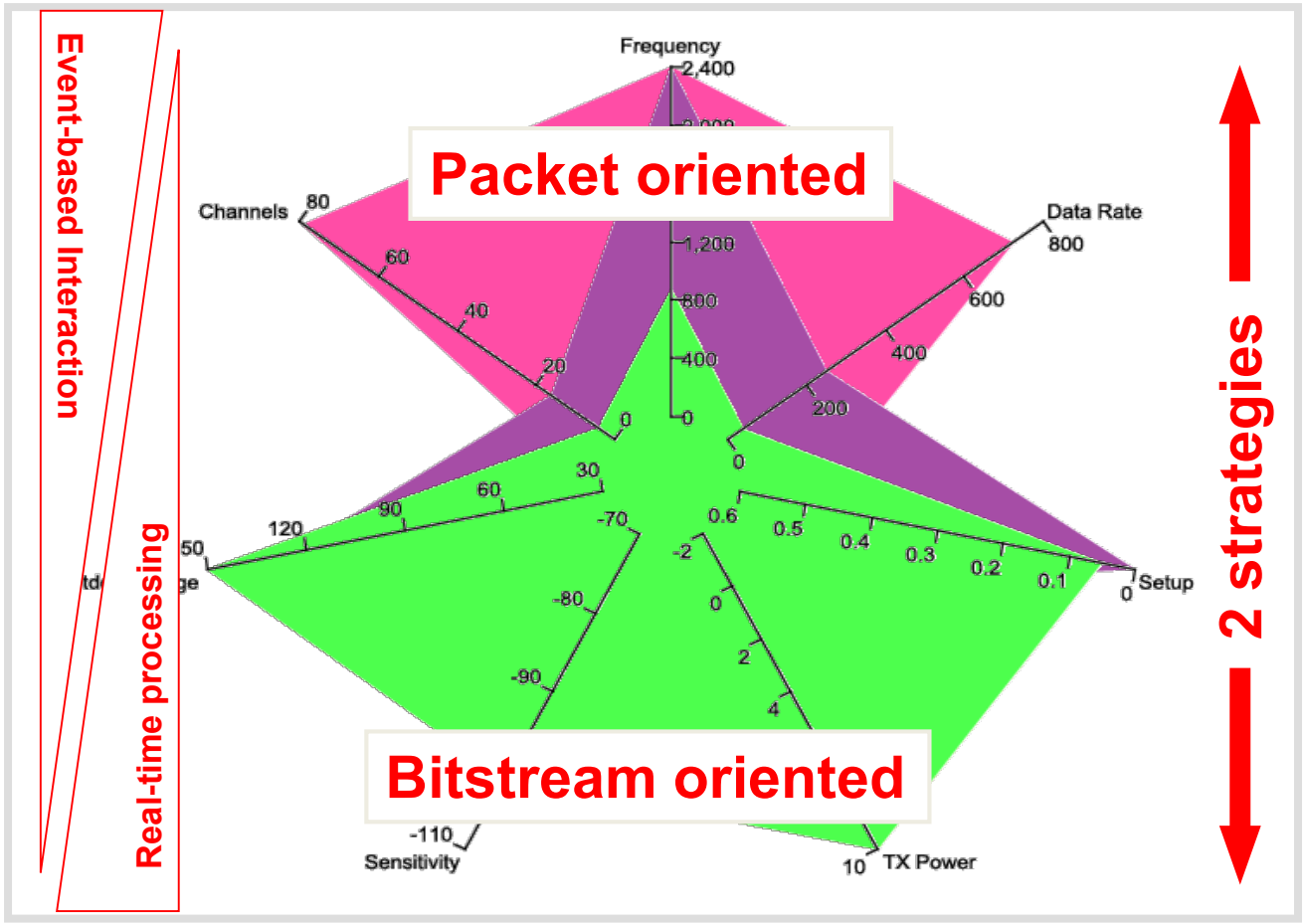
Comparing Radio Systems


Mica2


Mica2Dot


Tmote Sky

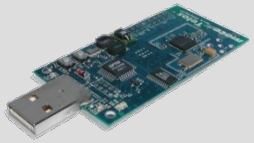

Imote



State-of-the-Art Platforms Comparison

Mica2

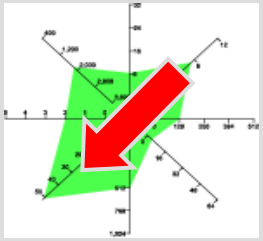
Mica2Dot

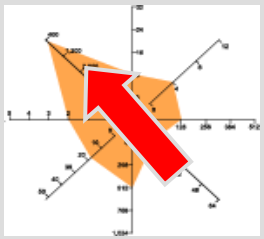


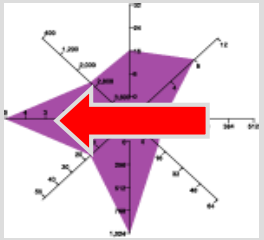
Tmote Sky

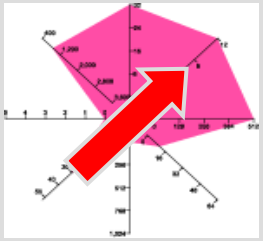
Imote

System Core

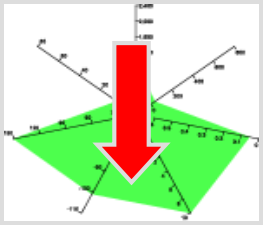


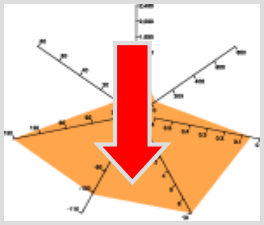


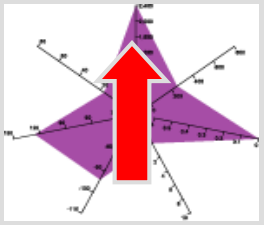


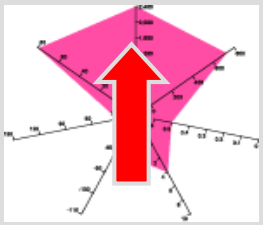


Radio Systems







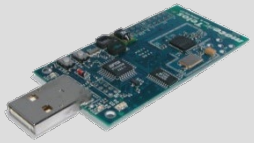


Bias towards a special purpose

State-of-the-Art Platforms Comparison

Mica2

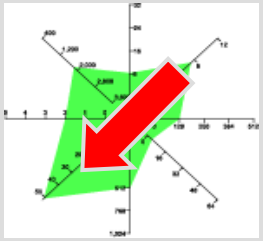
Mica2Dot

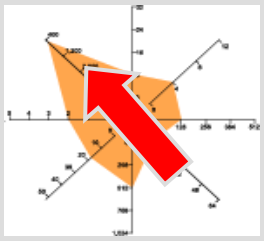


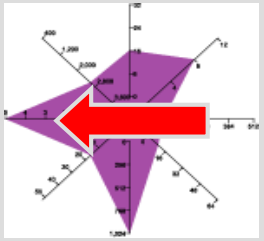
Tmote Sky

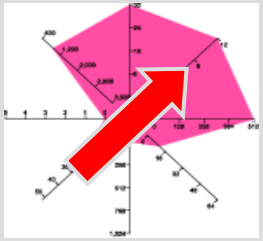
Imote

System Core

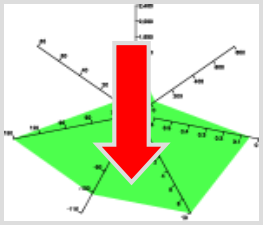


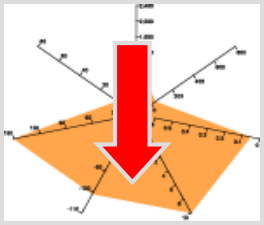


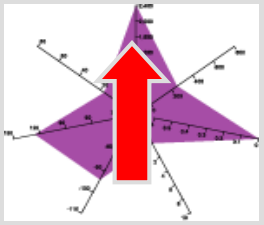


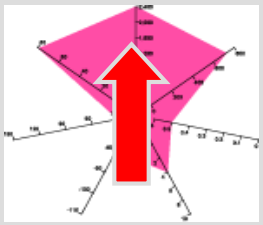


Radio Systems









Other platforms?

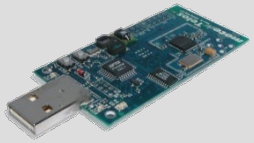
Balanced computing resources?

Multipurpose radio?

State-of-the-Art Platforms Comparison

Mica2

Mica2Dot

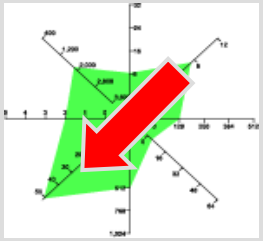


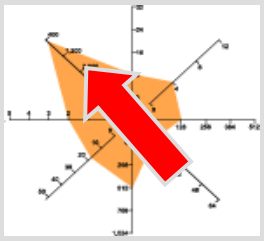
Tmote Sky

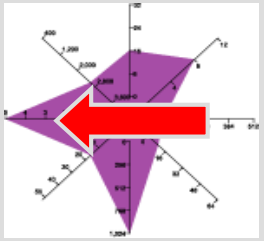
Imote

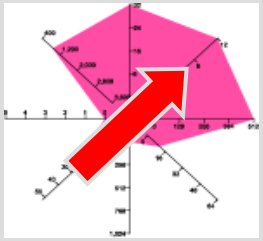
BTnode rev3

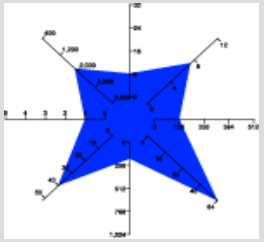
System Core



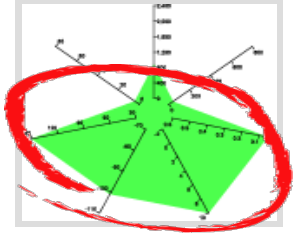


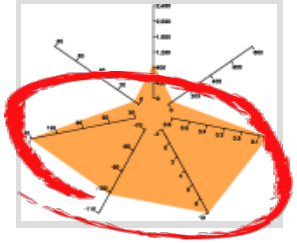


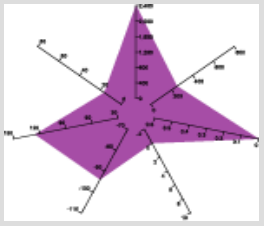


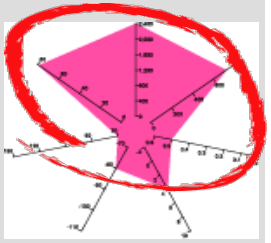


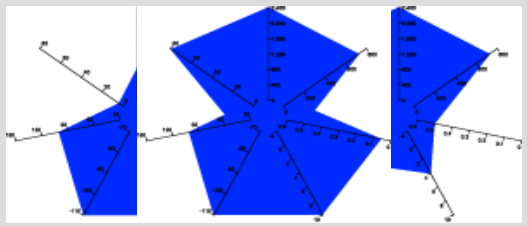
Radio Systems











Low-Power System Design

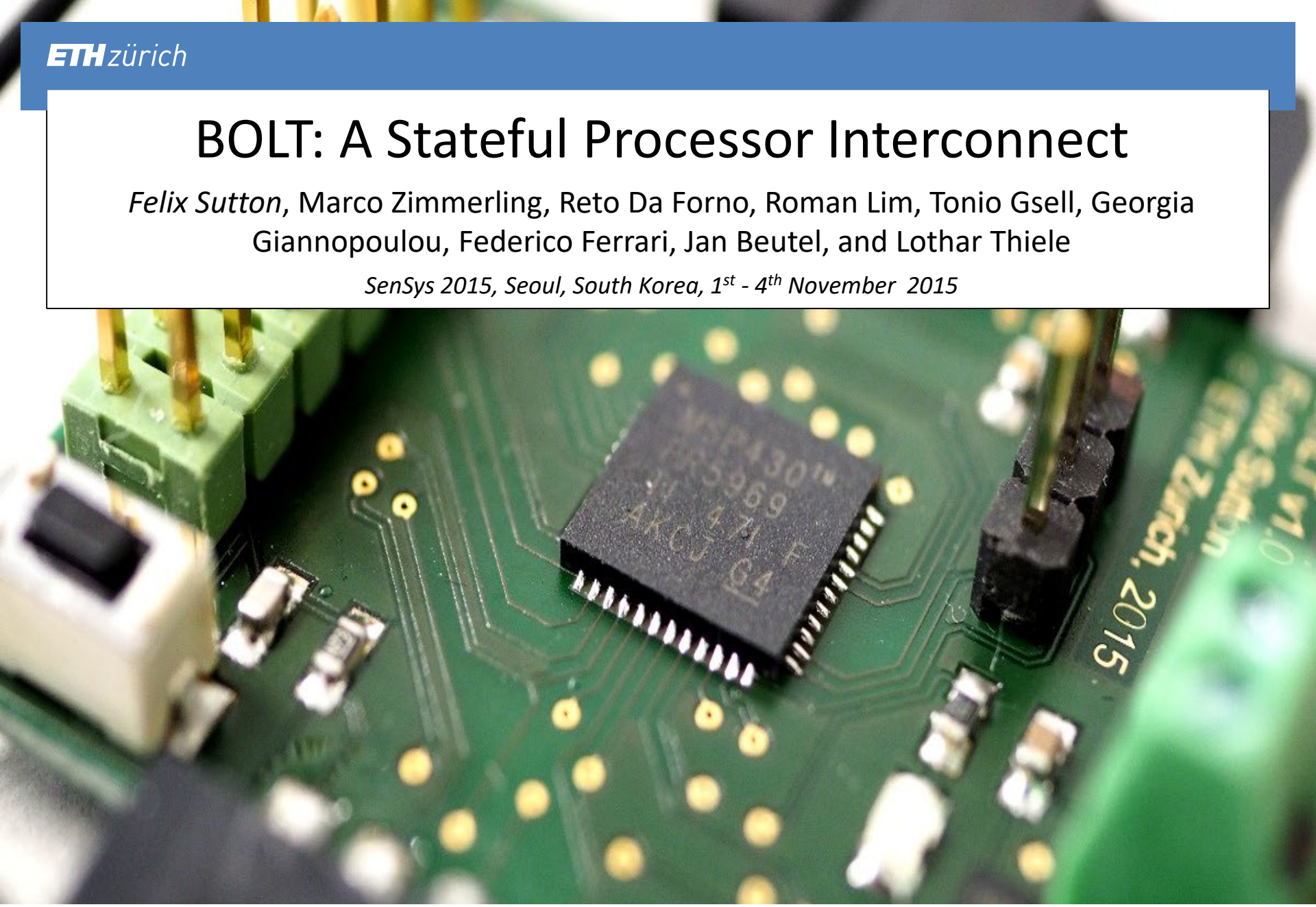
CURRENT RESEARCH EXAMPLE: MANAGING CONCURRENCY BY SEPARATING CONCERNS

ETH zürich

BOLT: A Stateful Processor Interconnect

Felix Sutton, Marco Zimmerling, Reto Da Forno, Roman Lim, Tonio Gsell, Georgia Giannopoulou, Federico Ferrari, Jan Beutel, and Lothar Thiele

SenSys 2015, Seoul, South Korea, 1st - 4th November 2015



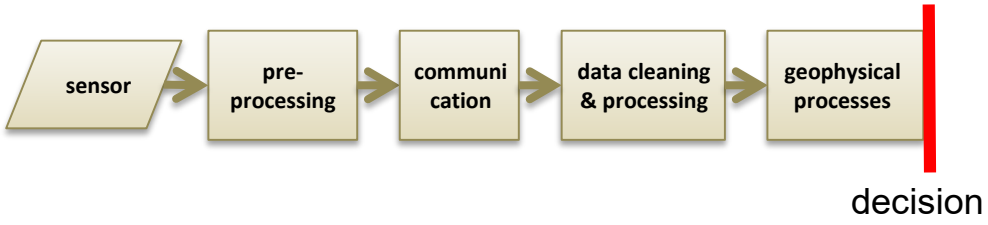
TIK Institut für Technische Informatik und Kommunikationsnetze

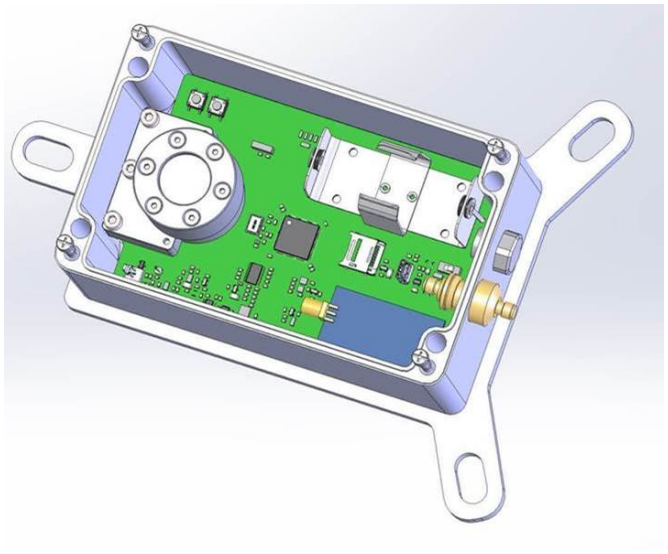
FNSNF

nano-tera.ch

“Intelligent” Triggered Sensors

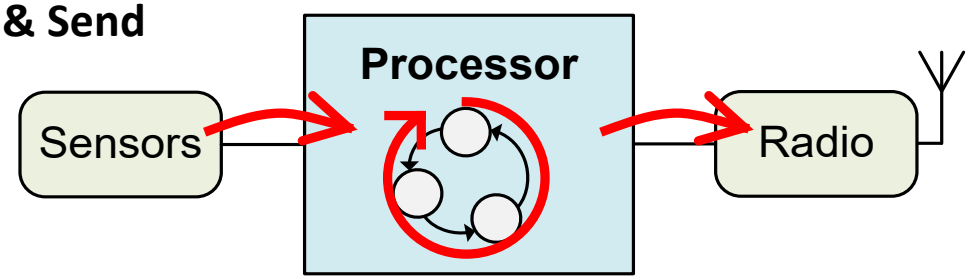
- Moving the decision into the sensor
- Asynchronous operation, jitter
- Data: Timing and event characteristics
- Co-detection over many sensors
- Less data, less power





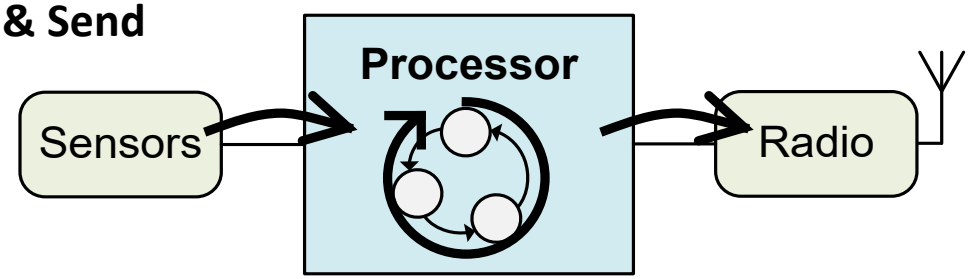
The Classical Mote

Periodic Sense & Send

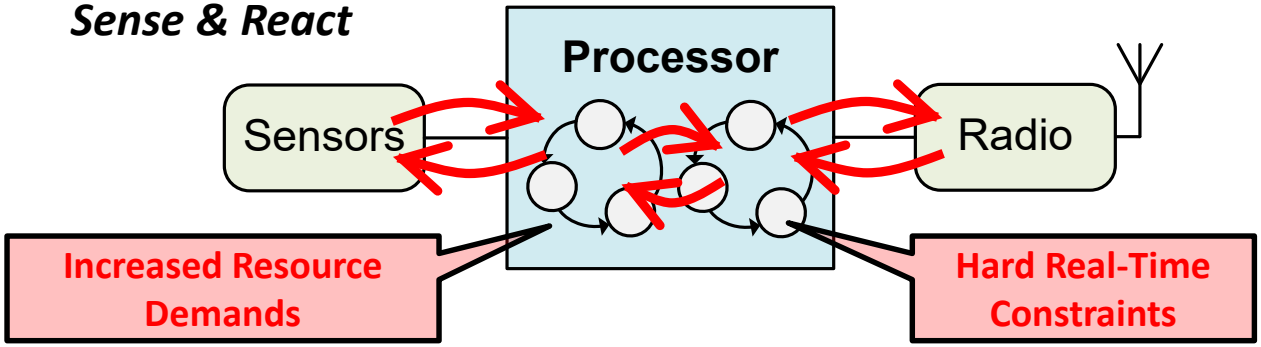


The Classical Mote

Periodic Sense & Send

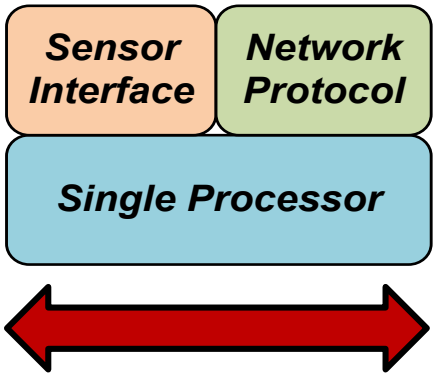


Sense & React



Revisiting Platform Design

Classic Architecture

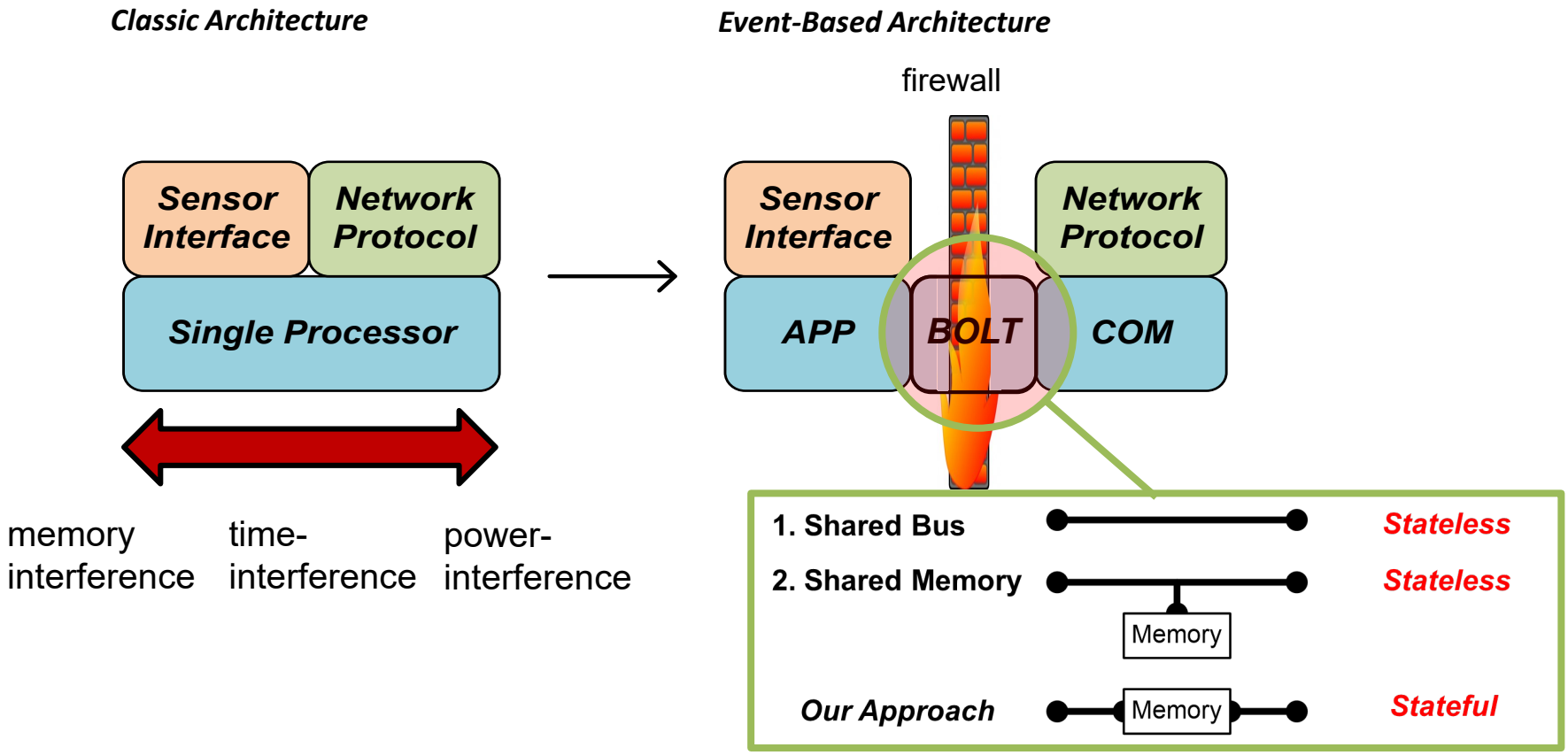


memory interference

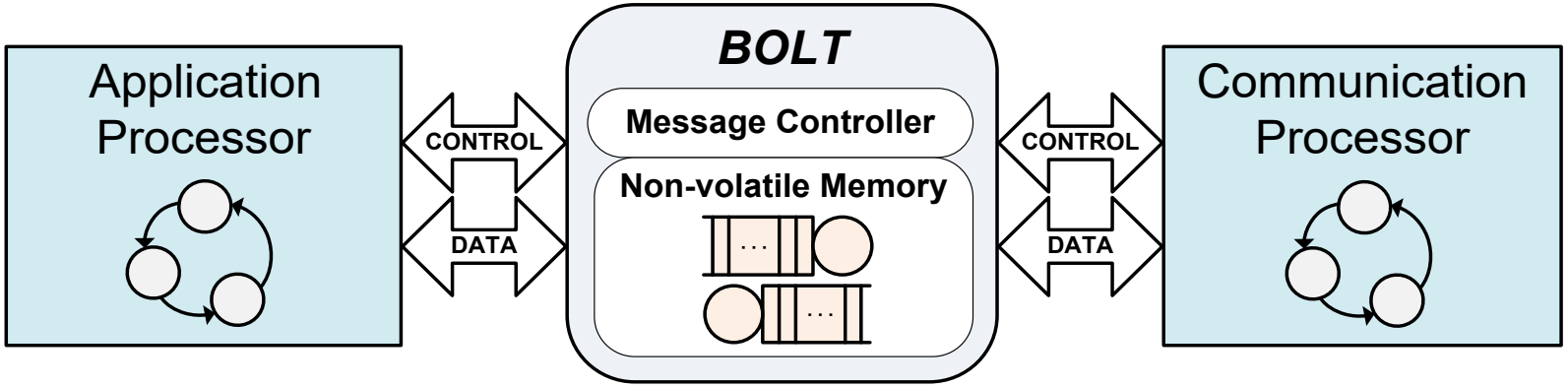
time-interference

power-interference

Revisiting Platform Design



BOLT: Ultra-low Power Processor Interconnect

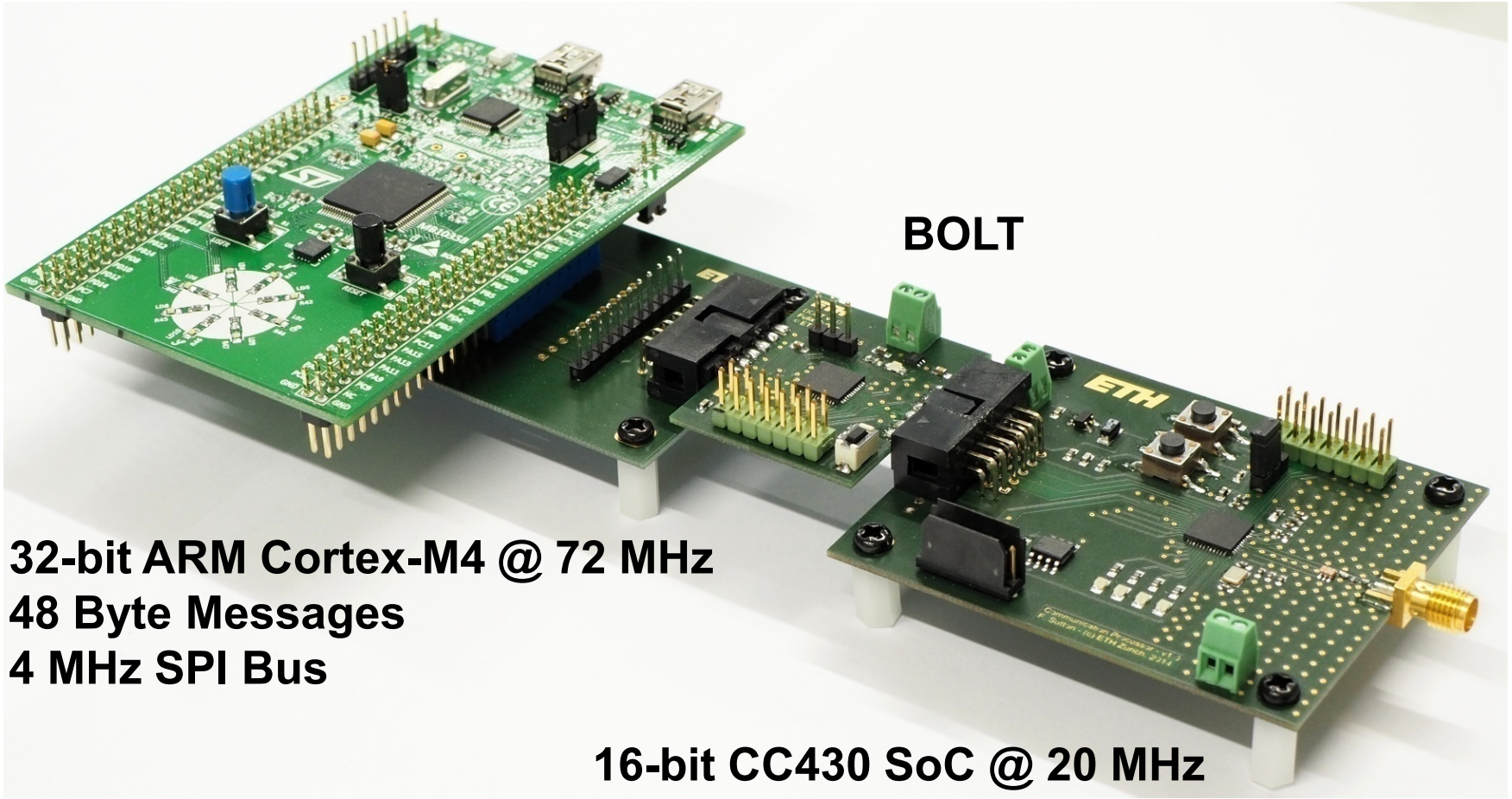


Design principles for predictable run-time behavior

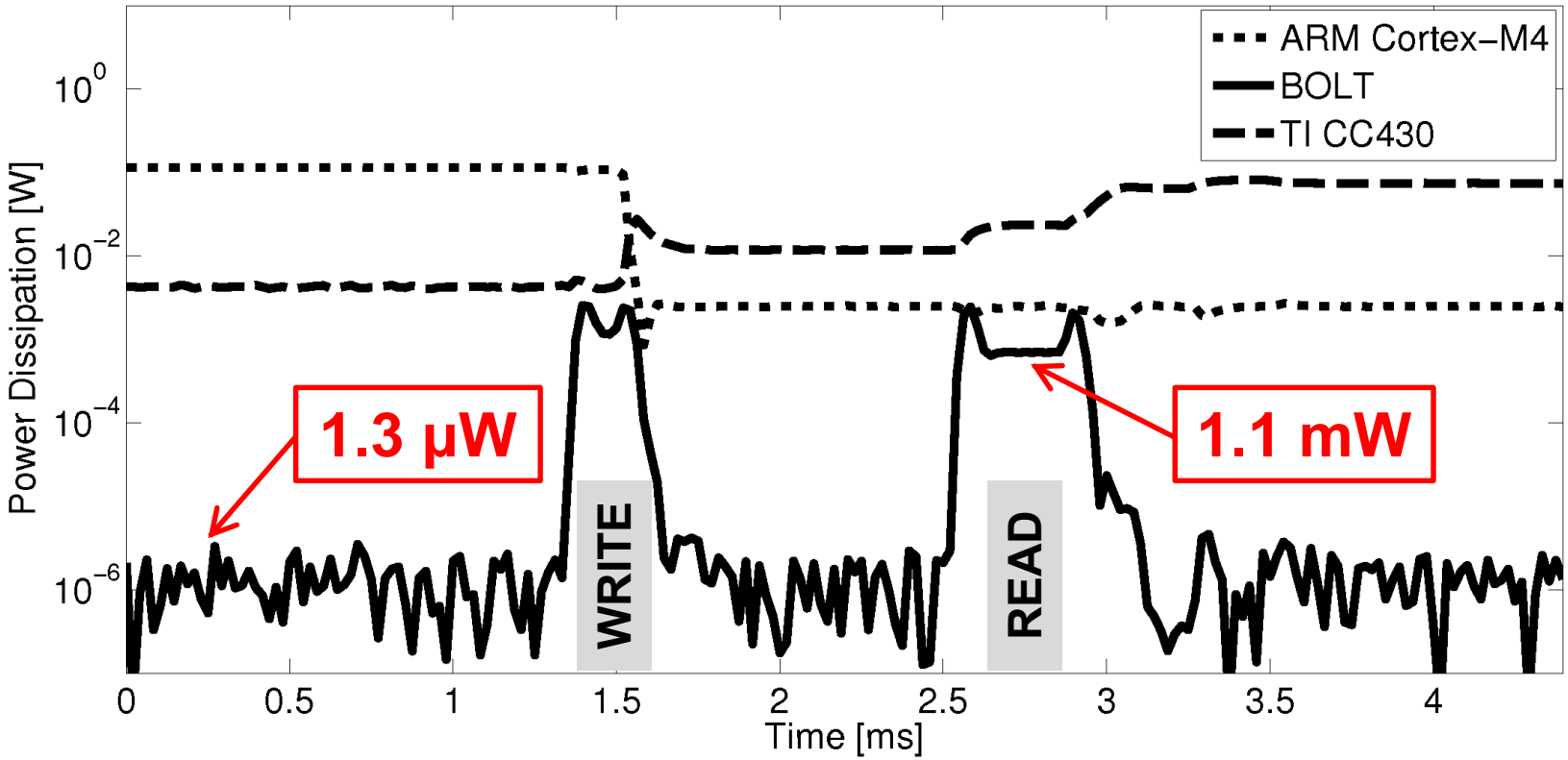
1. Avoid resource interference
2. Tightly bound unavoidable resource interference

[F. Sutton et.al.: *Bolt: A Stateful Processor Interconnect*. Proc. SenSys 2015]

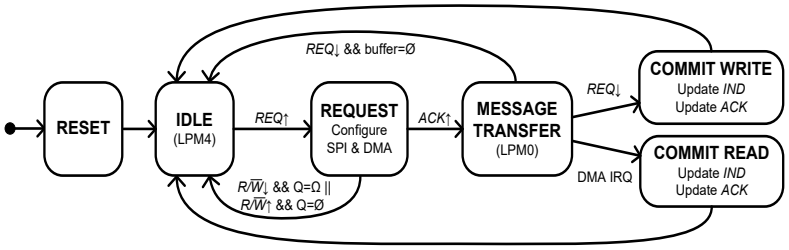
BOLT Prototype Case Study



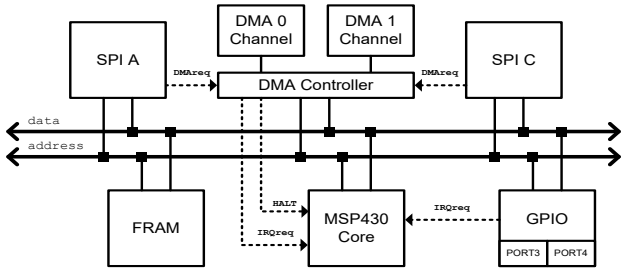
BOLT Power Dissipation



Bound Interference using a Formal Method

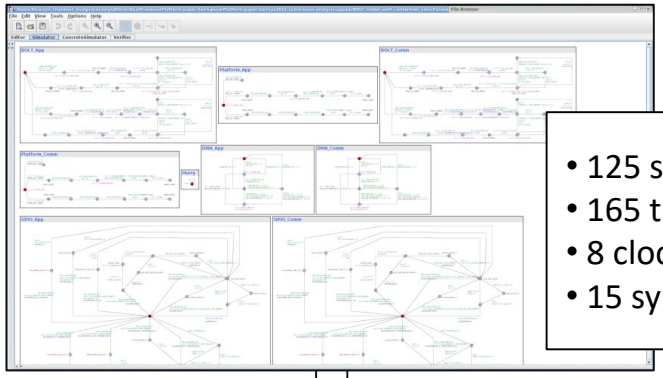


Software Model



Hardware Model

UPPAAL
Timed Automata
Model Checker

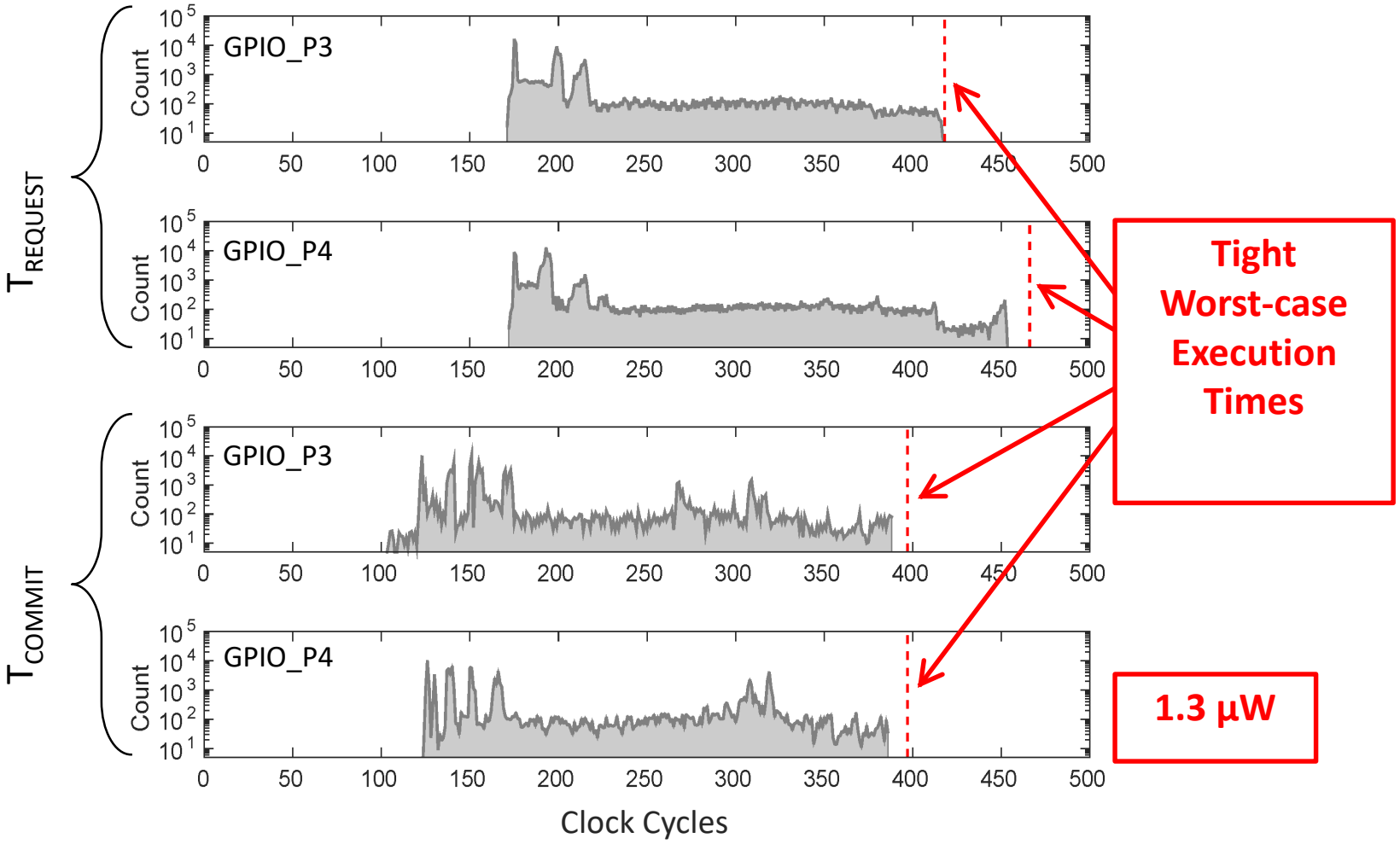


- 125 states
- 165 transitions
- 8 clock variables
- 15 sync channels

Worst-case Execution Time

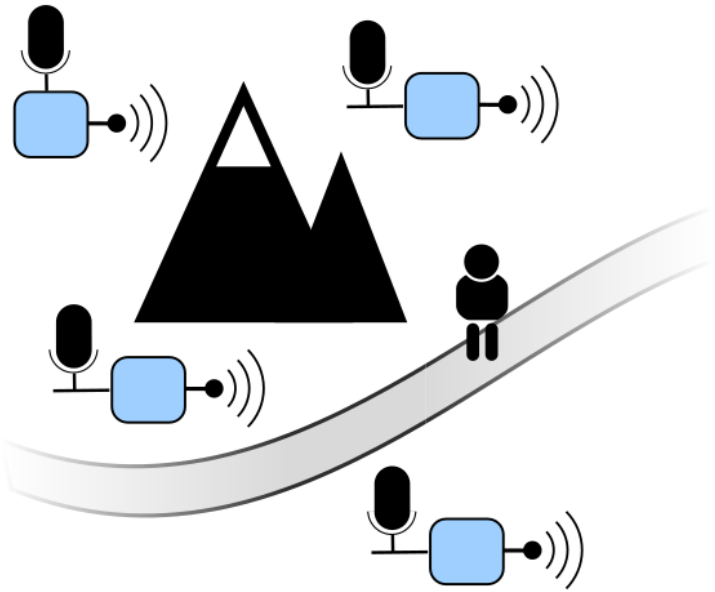
[F. Sutton et.al.: *Bolt: A Stateful Processor Interconnect*. Proc. SenSys 2015]

Measurement of BOLT Predictability

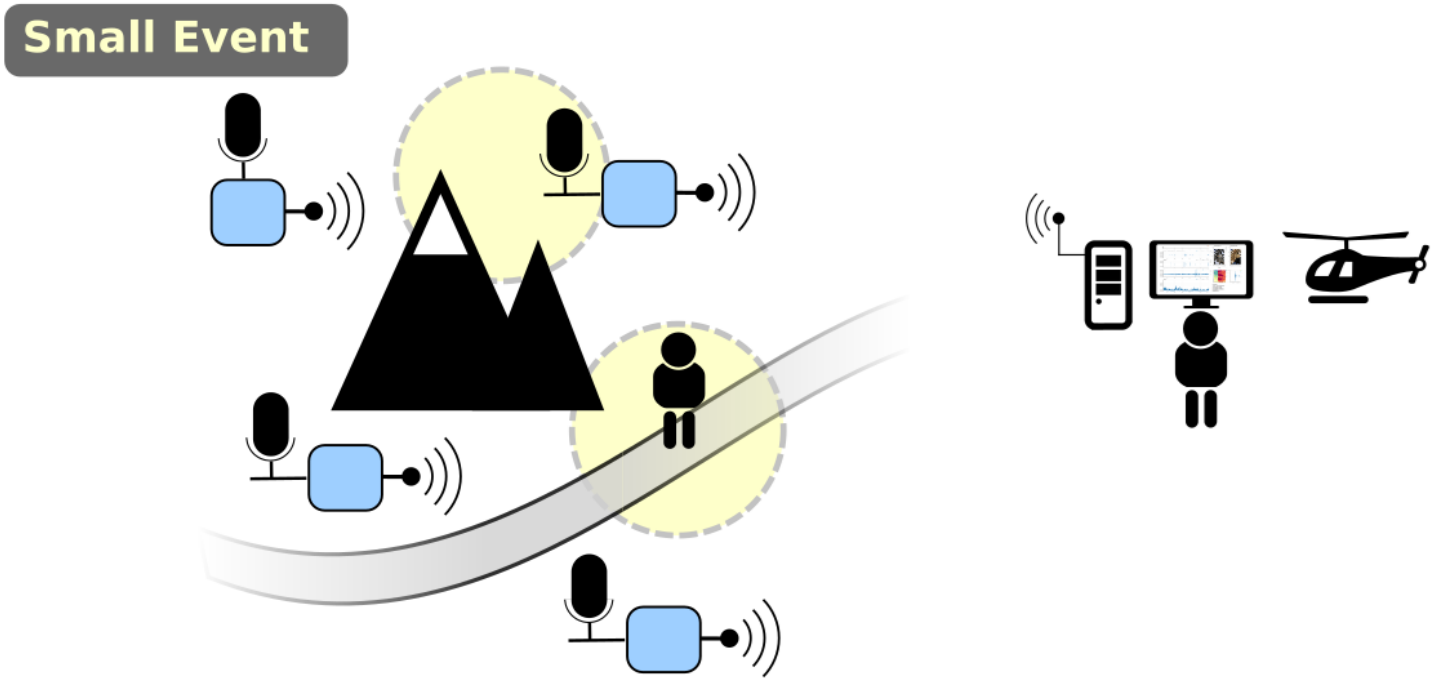


[F. Sutton et.al.: *Bolt: A Stateful Processor Interconnect*. Proc. SenSys 2015]

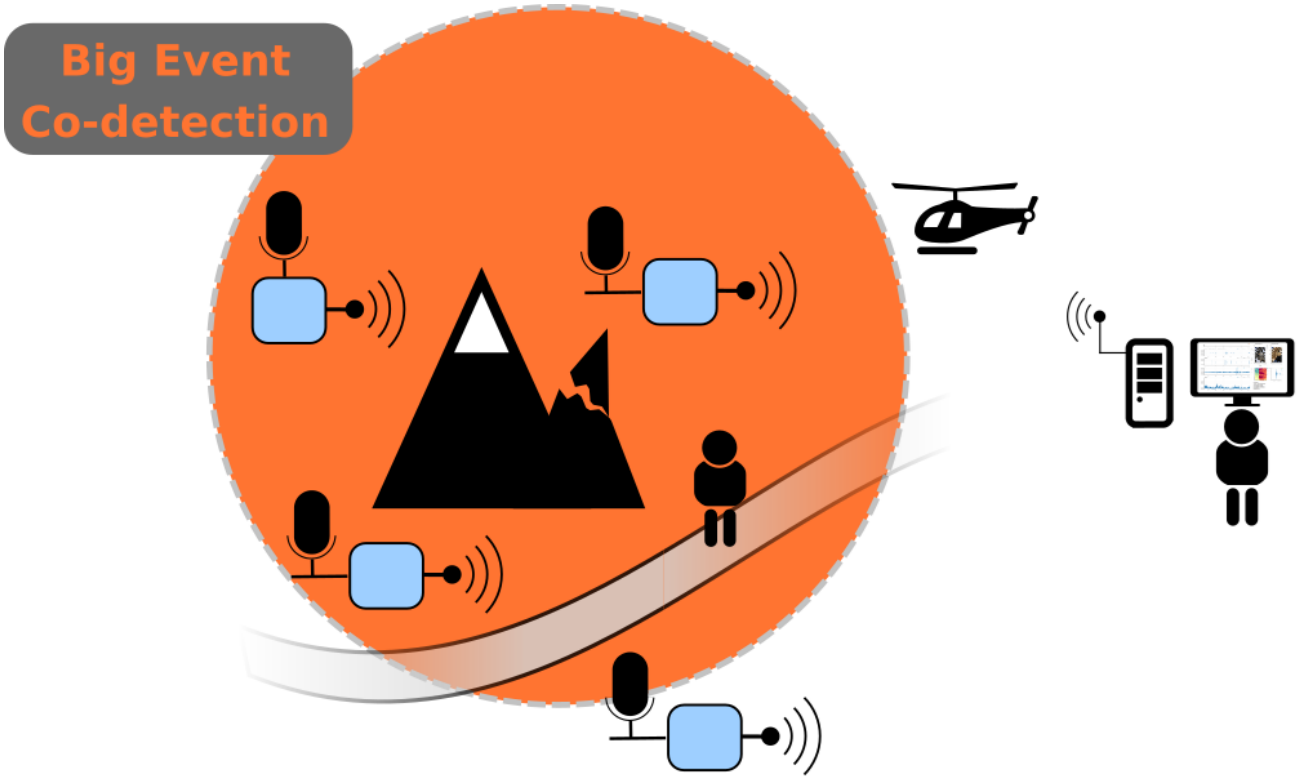
Application:
Co-detection of Seismic Events



Application:
Co-detection of Seismic Events

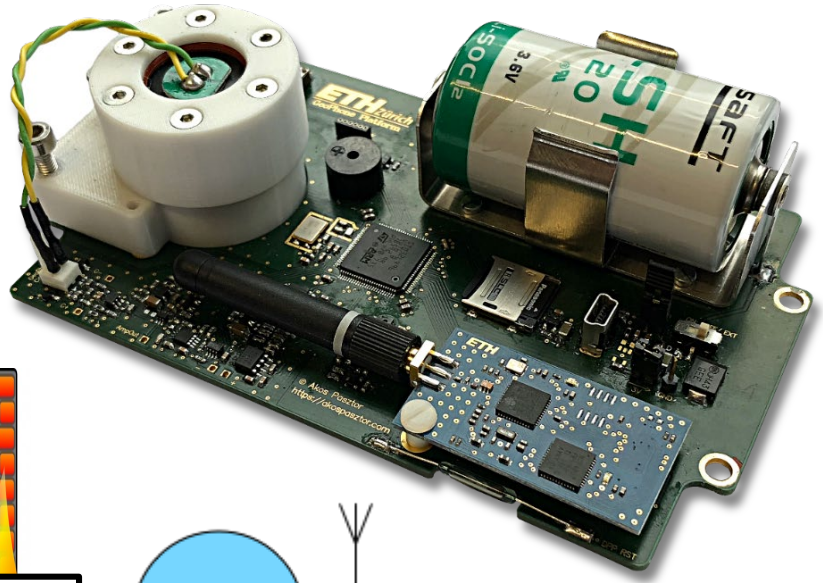


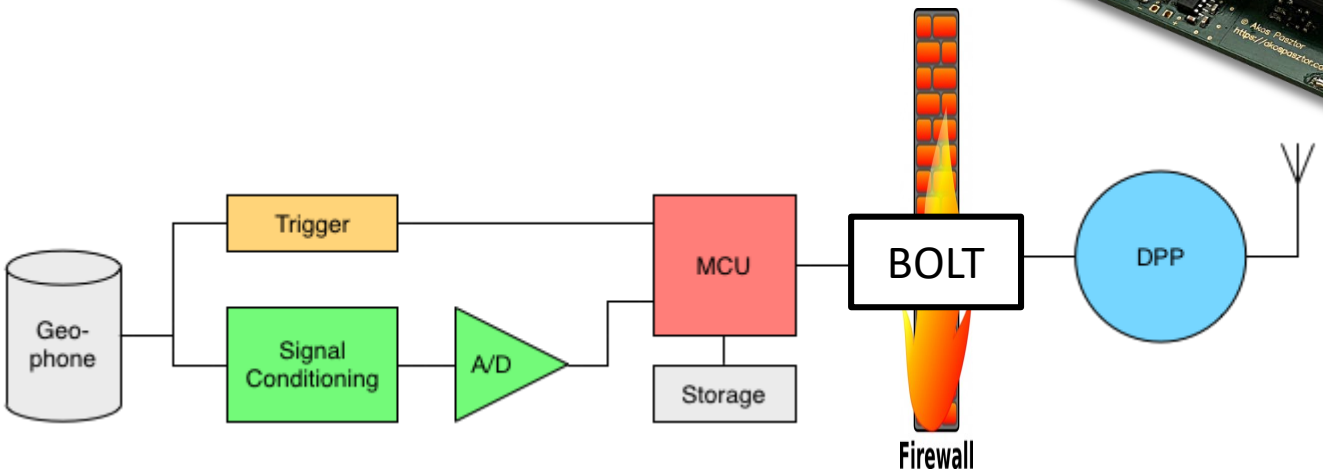
Application:
Co-detection of Seismic Events



Platform: Triggered Micro-Seismic Sensor

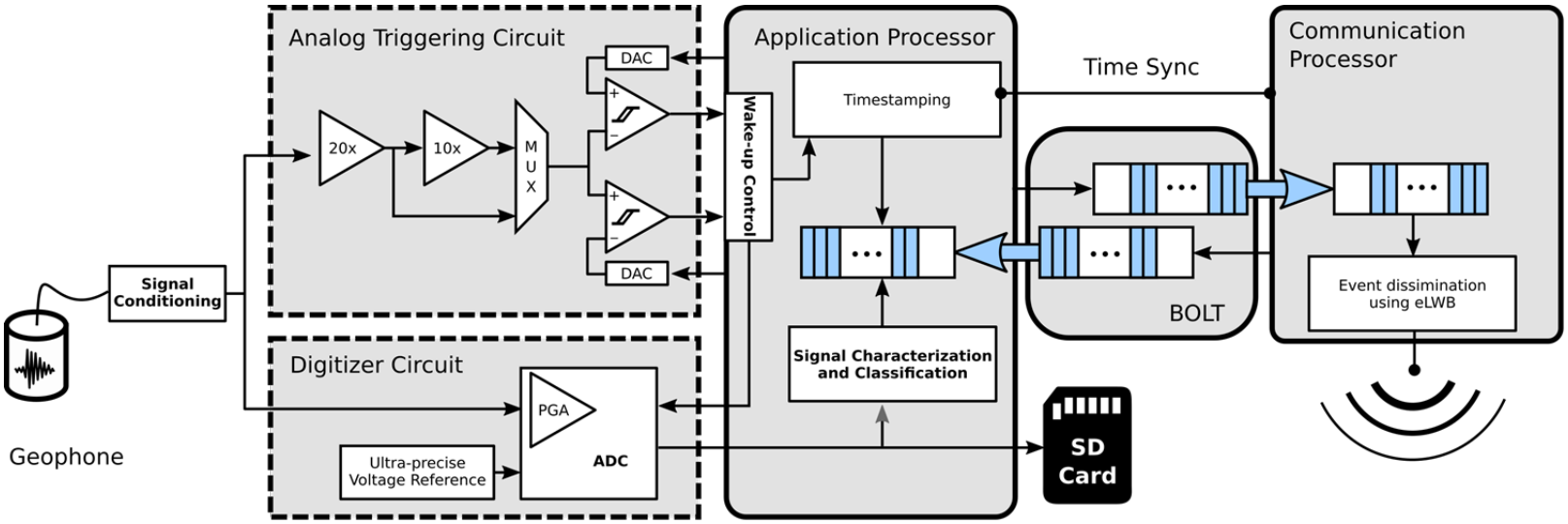
- Continuously active acoustic trigger:
  - 25 µA @ 3.0V
  - 50 µV sensitivity
- Wake-up latency <2.7 msec
  - 24-bit ADC, 140dB dynamic range
  - STM32L4 ARM Cortex-M4





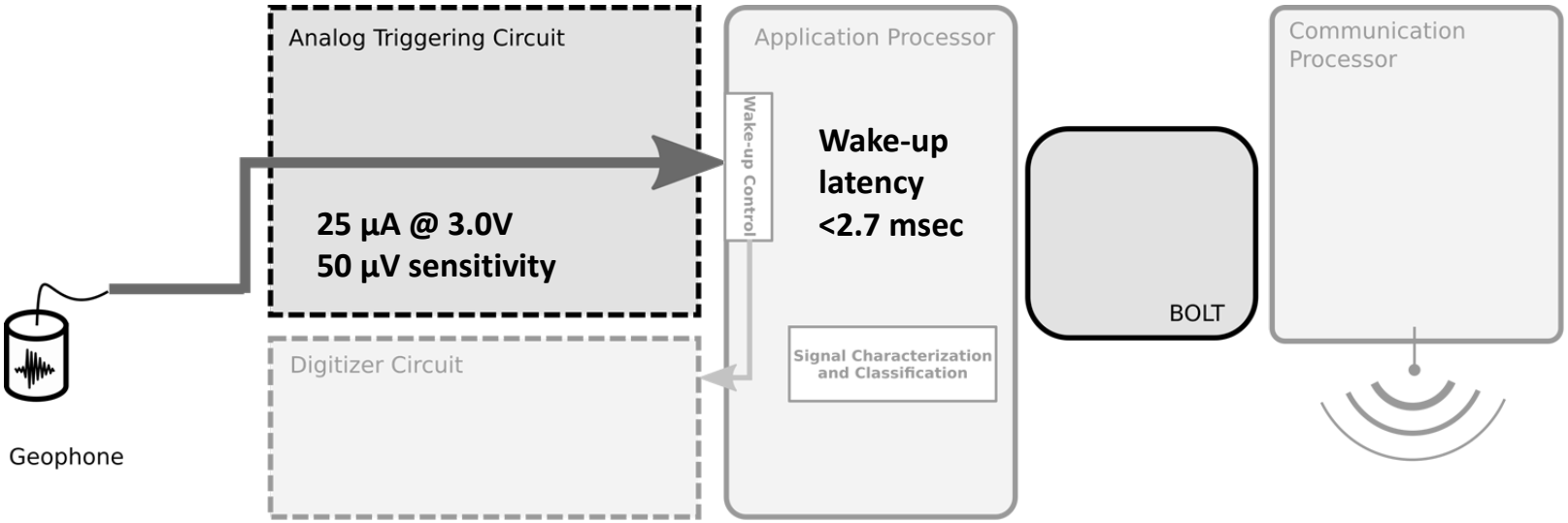
[A. Pasztor: *Event-based Geophone Platform with Co-detection*. MA Thesis, ETH Zurich, 2018]

Platform:
Triggered Micro-Seismic Sensor

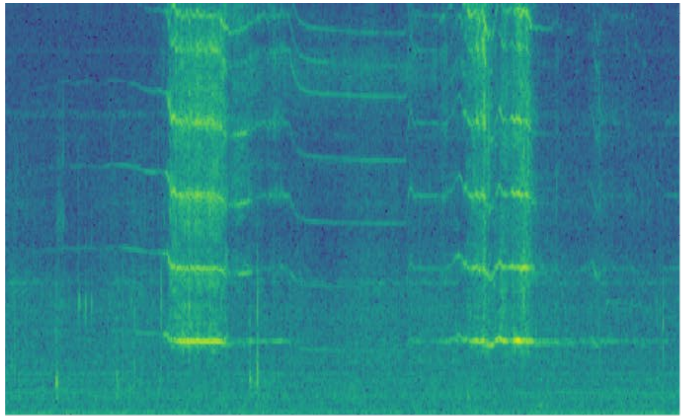


[M. Meyer et.al.: *Event-triggered Natural Hazard Monitoring with Convolutional Neural Networks on the Edge*. IPSN 2018.]

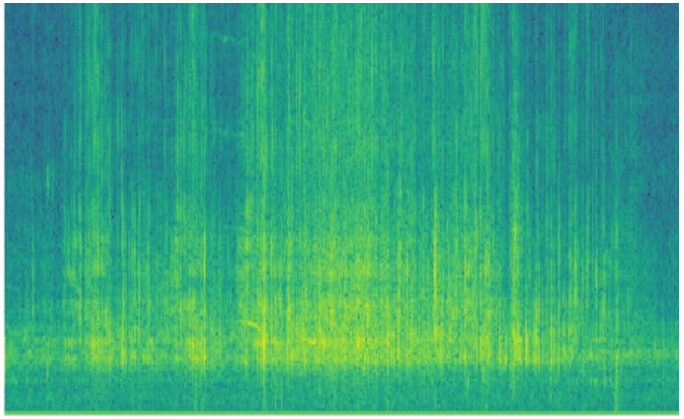
Continuously Active Seismic Wake-up Trigger



Which Signals Originate Within the Mountain



No Mountaineer



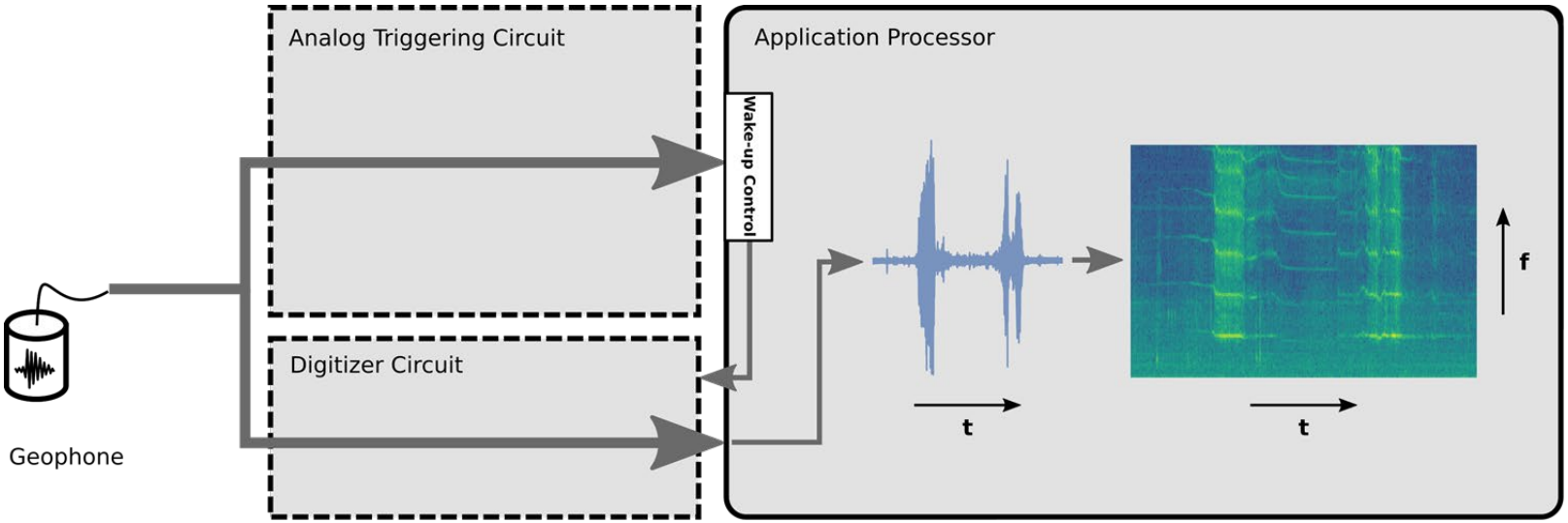
Mountaineer

[S. Weber, J. Faillettaz, M. Meyer, J. Beutel, A. Vieli: *Acoustic and micro-seismic characterization in steep bedrock permafrost on Matterhorn (CH)*. Journal of Geophysical Research: Earth Surface, 2018.

M. Meyer, J. Beutel and L. Thiele: *Unsupervised Feature Learning for Audio Analysis.* Proc. Conf. Learning Representations, April 2017.

Meyer, M., Weber, S., Beutel, J., and Thiele, L.: *Systematic Identification of External Influences in Multi-Year Micro-Seismic Recordings Using Convolutional Neural Networks*, Earth Surf. Dynam. 2018.]

On-board Signal Classification Using ML



Today's Hot Researcher & Paper

- Giovanni De Micheli
  - Faculty at EPFL
  - Previously faculty at Stanford University

- Very strong Influence in SoC and NoC paradigm
  - Prevailing hardware concept on today's embedded systems and mixed/multi-core systems implementations
- System-level dynamic power management with L. Benini (ETHZ)

L. Benini, G. De Micheli: *Networks on chips: a new SoC paradigm.* Computer 35 (1), 70-78

Recap of Today

- **Modern embedded hardware** (equally for high performance SoCs) offer a **great feature set**
  - Many integrated peripherals/options
  - Meticulous **attention to power performance in all operating modes**

- **Software** control is **increasingly difficult**
  - Lack of support by design flow/tools for hardware specifics
  - Overall system complexity

- **Profiling methods necessary** to assess system level performance
  - Detailed figures in documentations work only for each unique case
  - Modeling capabilities are limited (we will discuss this in detail)